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## PCI EXPRESS CONTENDS FOR COMMUNICATIONS ROLE Page 50

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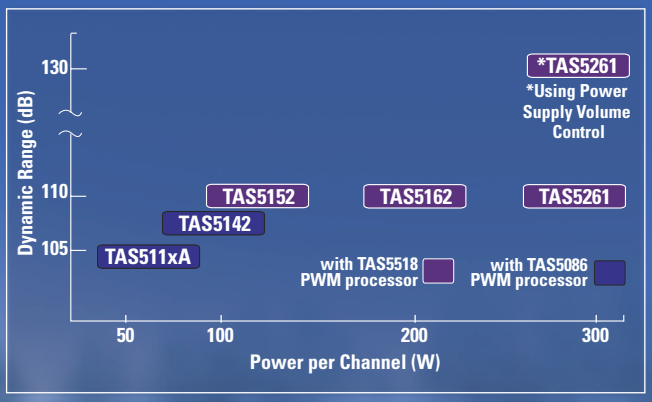




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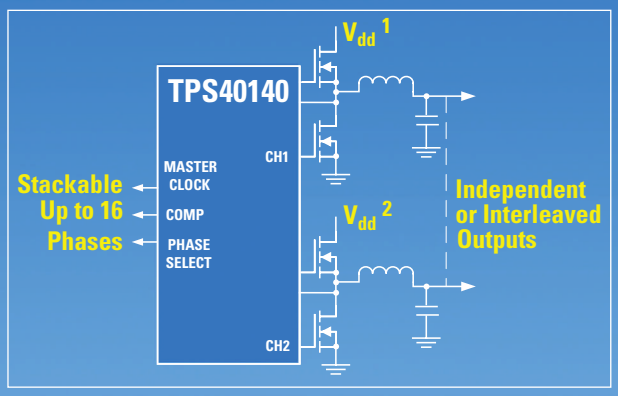


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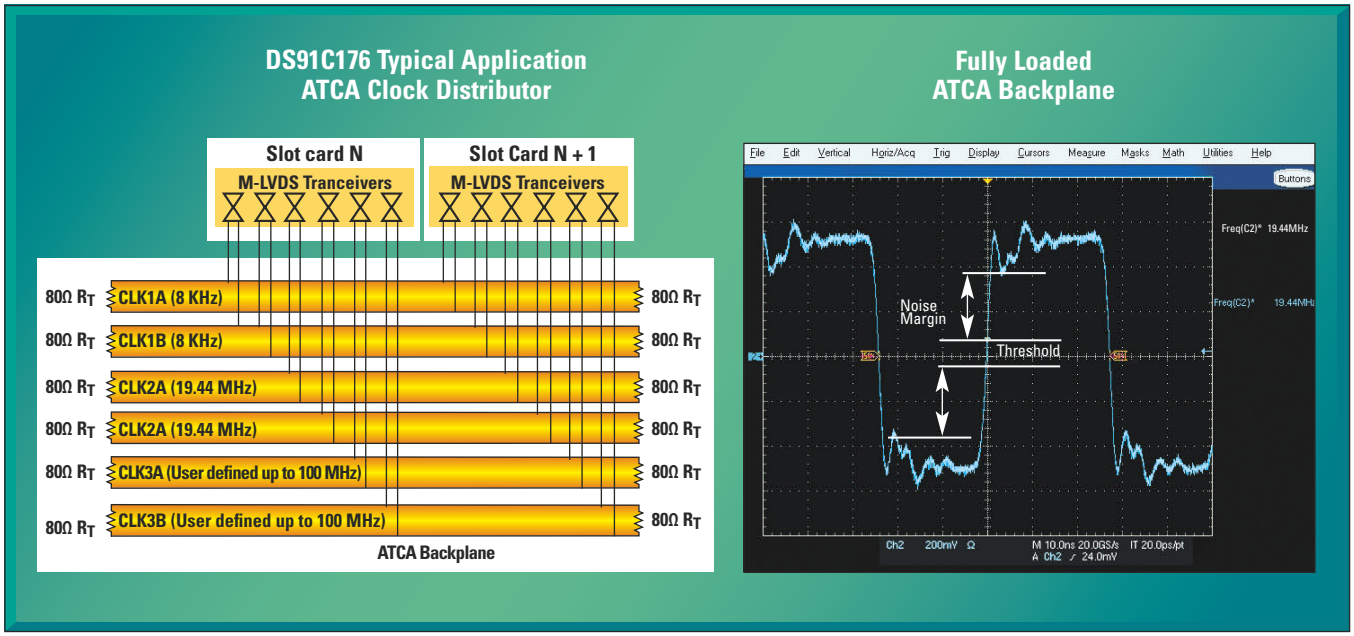


### Features

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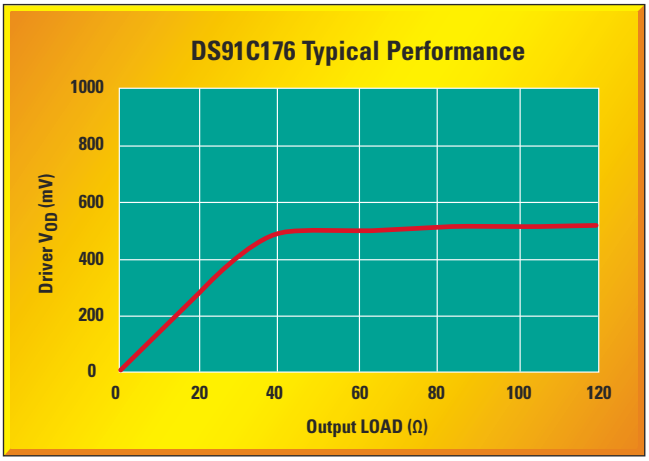


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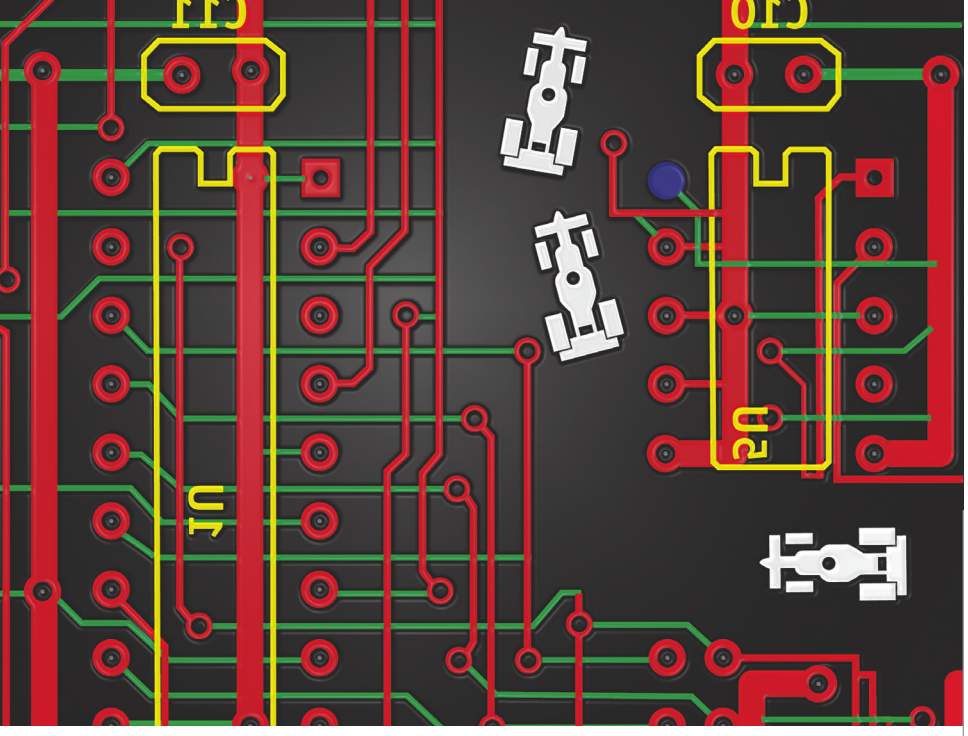

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50 years

# contents

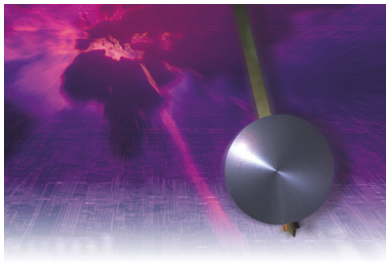
10.12.06

## PCI Express contends for communications role



## DLNA and HANA: two visions of consumer multimedia networking





## ASIC-design managers face global challenges



## Formal techniques solidify power-grid verification



## Quiet-node current sensing tames noise problems



## Maintaining channel compliance in high-speed backplanes



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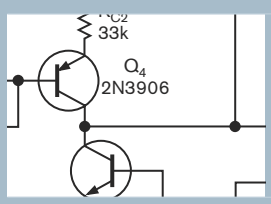




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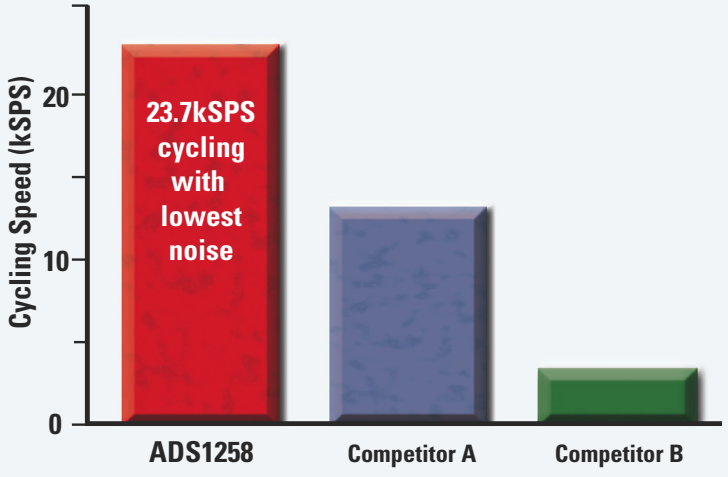
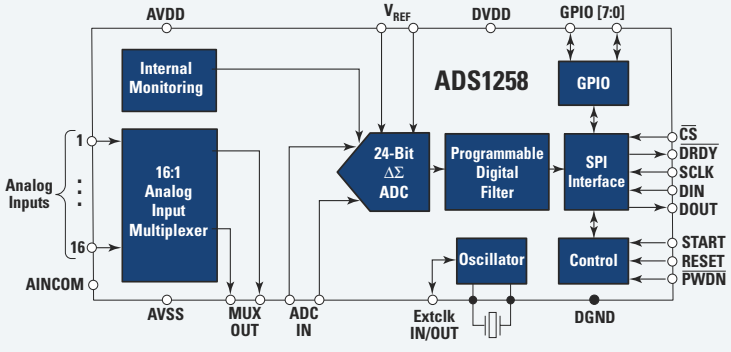
# Fastest Cycling 24-Bit ADC




The **ADS1258** 16-channel, 24-bit ADC from Texas Instruments features the lowest latency, fastest channel cycle rate and lowest noise of any competitive devices. With a measurement latency of 42µs, the ADS1258 can measure all of its 16 input channels in less than 675µs with only 12µVrms of input referred noise, offering unmatched performance for precision, multi-channel data acquisition applications.

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- Data acquisition
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- Instrumentation

## ▶ Features

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- Measure all 16 inputs in only 675µs
- Programmable digital filter 2.8µVrms noise at 1.8kSPS data rate
- Unipolar (+5V) or bipolar (±2.5V) operation
- INL: 0.0010% (max)
- Offset drift: 0.1µV/°C
- Package: QFN-48
- Pricing: $7.95 in 1k units

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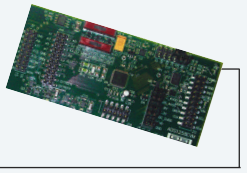

**www.ti.com/ads1258 ◦ 800.477.8924, ext. 13497**

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TEXAS INSTRUMENTS

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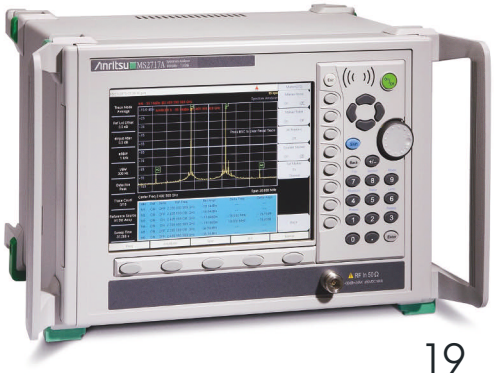
## pulse

Dilbert 20



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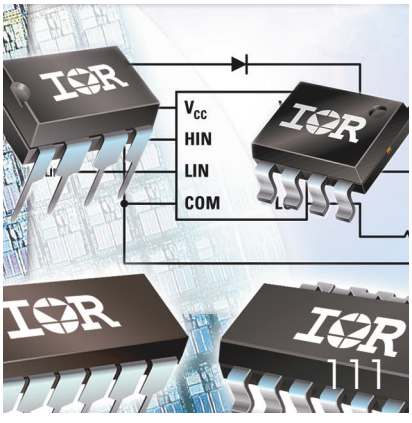


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## PRODUCT ROUNDUP




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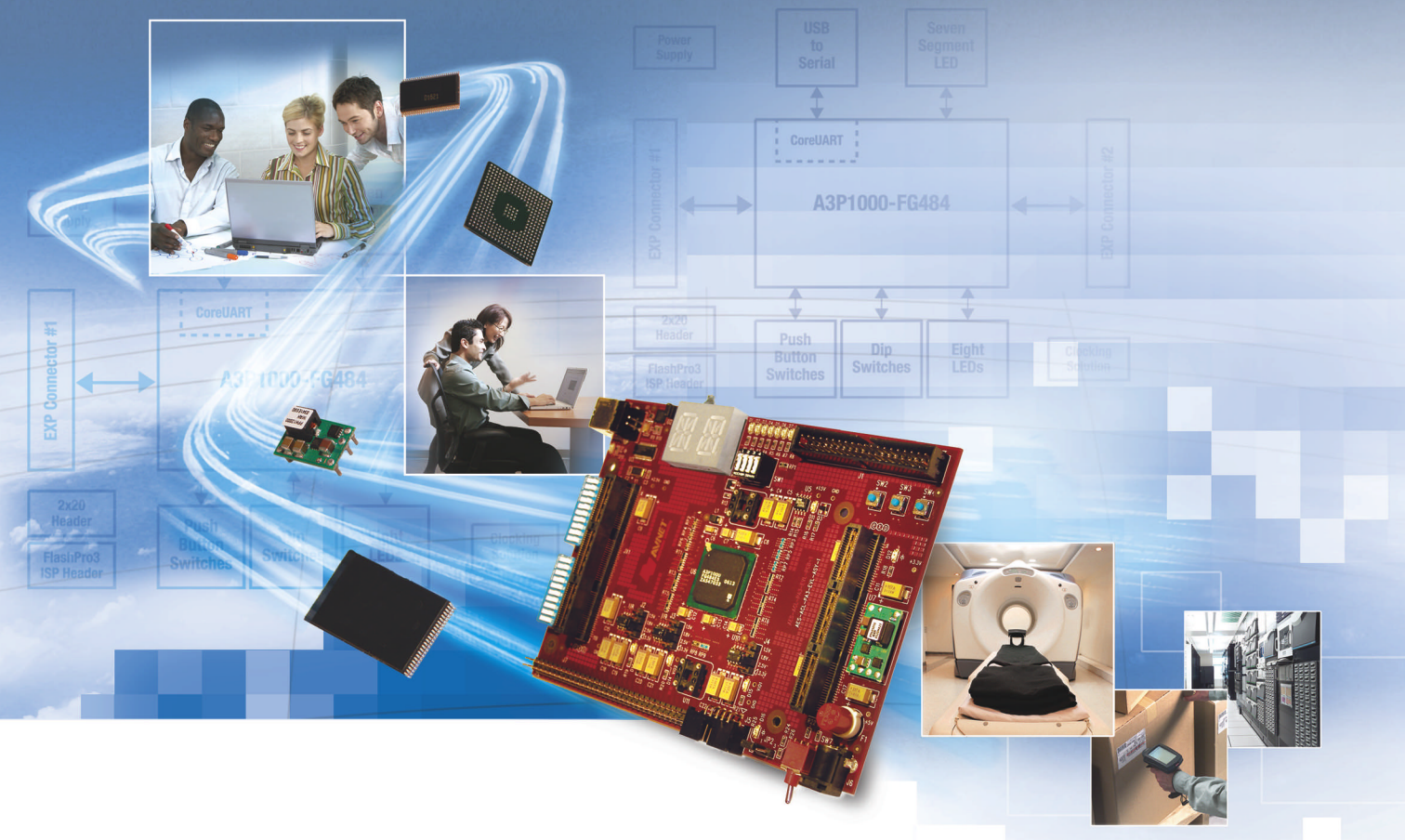


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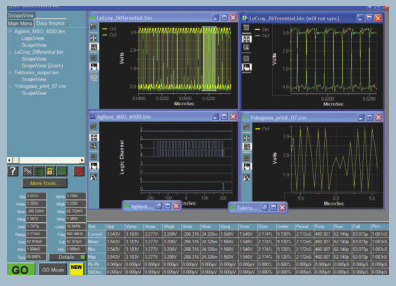

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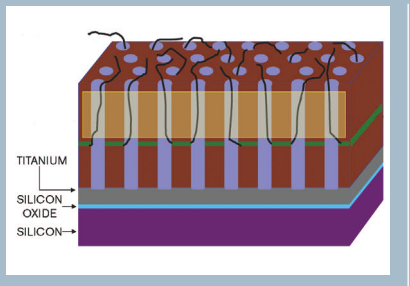


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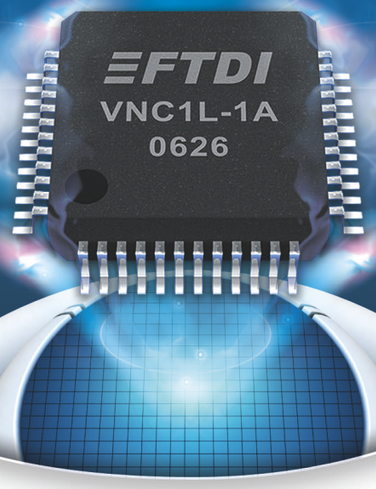


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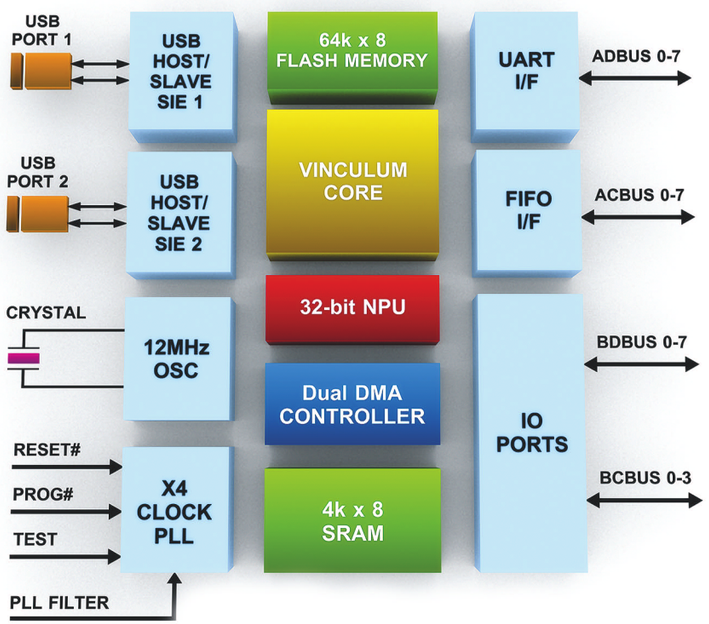
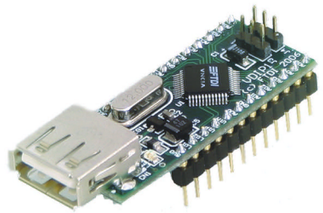
- Camera
- PDA
- Mobile Phone




WITH

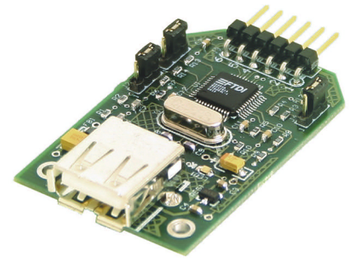
- MCU
- Serial Port
- USB Drive
- Kbd/Mouse

## Vinculum Evaluation Modules & Application Areas



The **VDIP1** module is an MCU to USB Host Controller development module for the VNC1L device and is ideal for rapid prototyping and development of VNC1L designs.

- Jumper selectable UART, SPI or FIFO MCU Interfaces
- USB "A" type socket to interface with USB peripherals
- 2nd USB Interface available via module pins if required
- Single 5V supply input
- Auxiliary 3.3V/200mA power output to power external logic
- Traffic Indicator LEDs



**VDRIVE1** is possibly the easiest solution for adding a USB Flash Drive interface to existing products. Only four signal lines plus 5V/GND are required to be connected.

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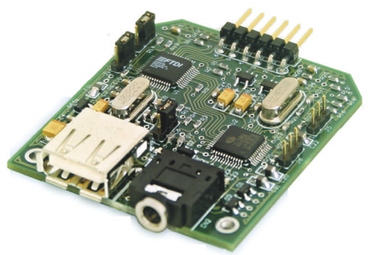
- Only 4 signals to connect excluding PWR/GND
- Single 5V supply required
- Easy to implement command set



**VMUSIC1** is a product that not only lets you add USB Flash Drive interfacing to your product but allows you to play back MP3 and other popular digital music formats direct from a USB Flash Drive.

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- Stereo 3.5mm headphone jack socket and audio line-out connector for audio playback.
- Link Selectable UART or SPI interface
- Only 4 signals to connect excluding PWR/GND
- Single 5V supply required
- Easy to implement command set

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BY MAURY WRIGHT, EDITOR IN CHIEF

# Triple-play trickery: Beware the buzzword bandwagon

Lately, it seems that almost every pitch I hear from marketers uses the term "triple play" in an attempt to leverage what they perceive as a hot market. But many of those pitchers don't even understand the meaning of "triple play," and most are stretching the truth more than a little in using it to describe their newest product. Now, I'm not the arbiter of how to use words. But I have followed the voice-, video-, and data-services market since before broadband data and digital video became realities. My point is to advise you to closely scrutinize anything that mentions "triple play" because I am increasingly finding that marketers are often using the hype to hide the lack of compelling features in products or to get publicity.

The term "triple play" implies a service offering from telecom carriers, MSOs (multiple systems operators), satellite operators, or maybe even power utilities. The term "triple" implies that the offering includes voice, video, and data services. The telecom carriers need the revenue from triple-play offerings to help cover the revenue shortfall they attribute to the commoditization of voice services. MSOs, at least in North America, are typically the incumbents in profitable video services and were the first to broadly offer broadband. You might think MSOs would want no part of the low-margin voice business, but, realistically, it costs almost nothing these days for them to add voice to their video and data offerings.

Triple-play offerings have attracted interest from analysts and other experts because the success of these offerings will go a long way in determining which carriers are still with us in a few years. Even the politicians have jumped on the bandwagon, as the telecom carriers strive to offer video without signing franchise agreements with communities, as MSOs must do.

Because you read so much about triple play, vendors of ICs, boards, and even cables or power supplies are using the term to promote their products. For example, the spin doctors label home-networking products as triple-play products. Perhaps home LANs will eventually find use in distributing video around homes, but none have yet proved capable. Moreover, some, such as power-line-based HomePlug technology, will probably never carry high-definition-quality video.

There's also hype aplenty from the communication-IC crowd. Vendors of everything from Ethernet switches and network processors to traffic managers and network-search engines trumpet triple-play capability. Some of these products may prove key enablers in network equipment that service providers rely on to offer the triple play. But most of the vendors claim that their chosen technology is the only avenue to the triple play. I'd argue again that triple play is simply a service offering and consumers don't care how carriers deliver it.

Recently, companies have been bombarding me with presentations on the theme of a converged network that carries video and voice over the same IP (Internet Protocol) transport-protocol device that delivers data. Now, I'm all for converged networks. I was editor of *CommVerge* magazine in the 1999 to 2002 time frame, and *CommVerge* focused on convergence. But we were wrong then about how quickly a converged network might become reality. And I'm still not sure how fast the carriers can broadly move to IPTV—especially when the requirement includes carrying multiple HDTV-quality streams.

Although current telecom networks aren't IPTV-capable, those networks aren't the biggest roadblock to triple-play offerings. The last mile remains the roadblock. As I recently chronicled, the carriers are just beginning to roll out IPTV-capable broadband pipes (**Reference 1**). The triple-play offerings now on the market almost universally rely on an overlay network to deliver the video. And no matter how many communication-IC vendors hype their triple-play ICs, carriers will not rip up core and access networks and install new ones unless the converged network can reach the home. Even if or when the carriers move to converged networks, they will be just that: multimedia-capable IP networks, not triple-play networks.

The carriers get it. They are even talking "quad-play," throwing mobile service into the bundle. And mobile services clearly don't arrive through a converged network. But the enabling-technology vendors will continue the hype. EDN

## REFERENCE

1 Wright, Maury, "100-Mbps broadband: How, why, when, and where?" *EDN*, July 6, 2006, pg 48, www.edn.com/article/CA6347250.

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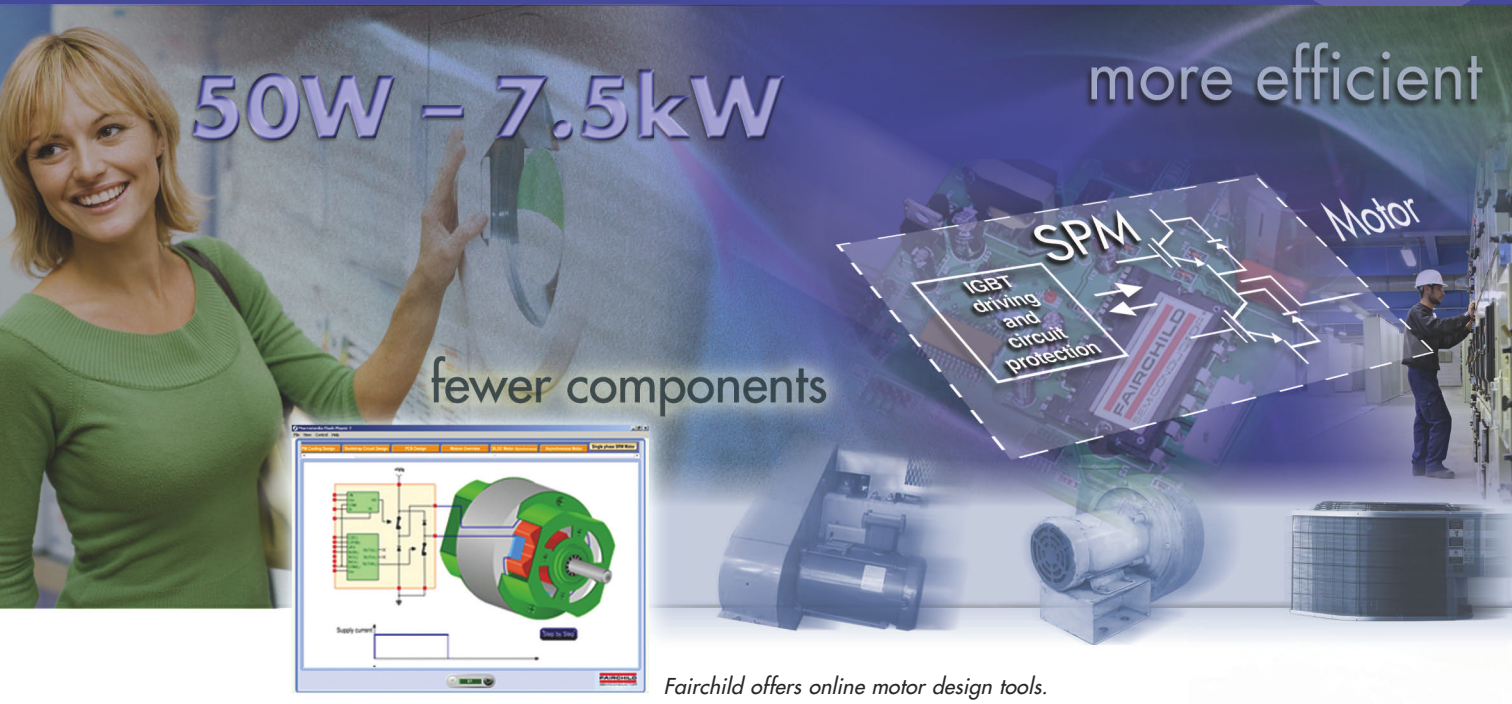


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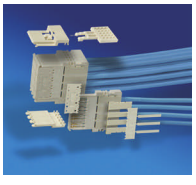

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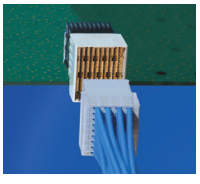
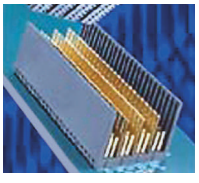


GORE™ EYE-OPENER® AirMax VS® Cable Assemblies



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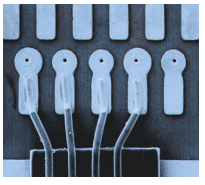

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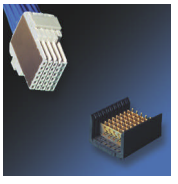

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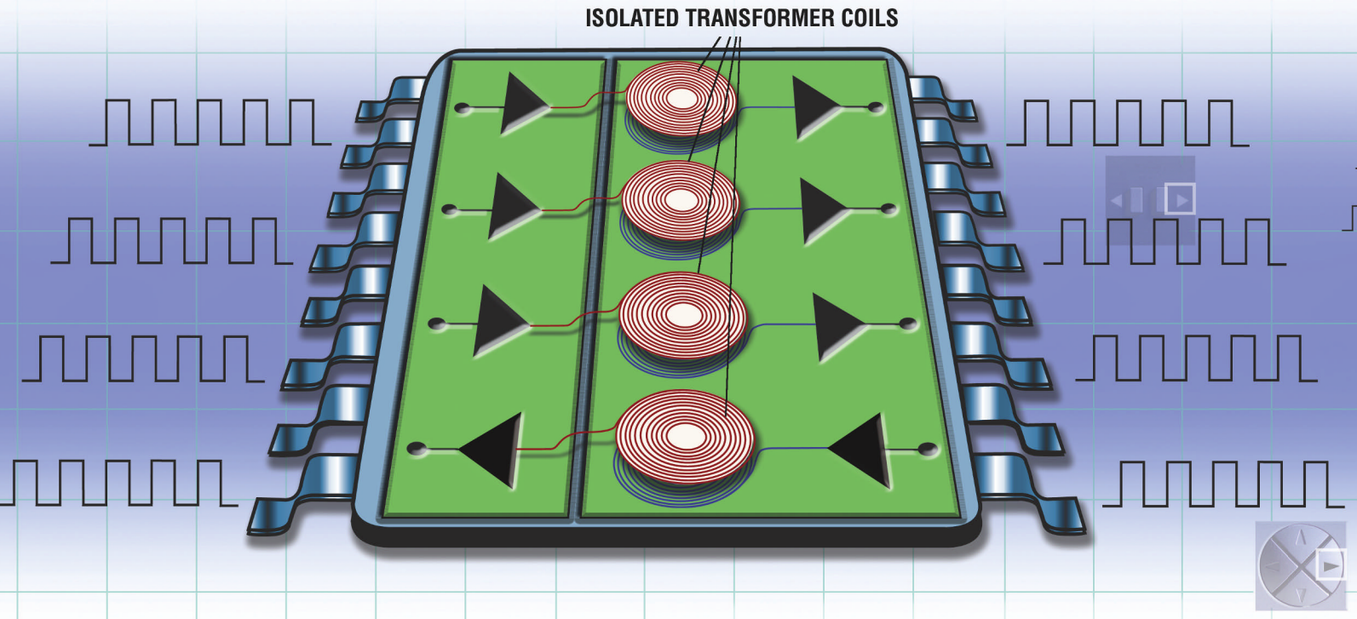


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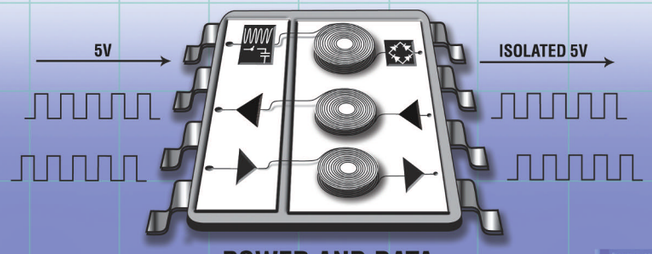


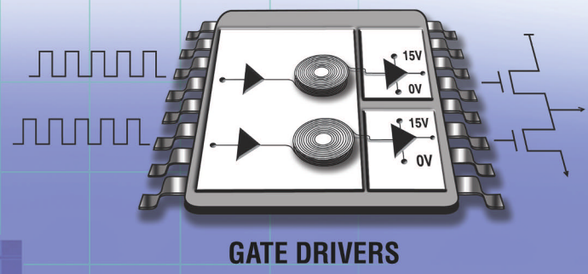


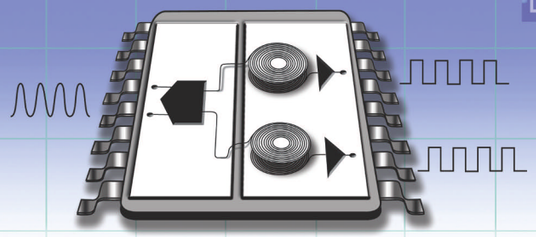


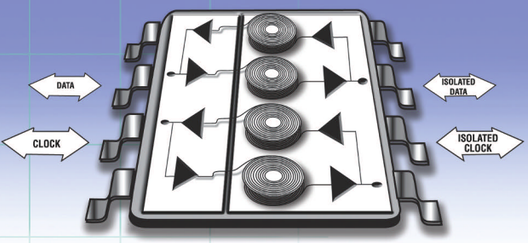


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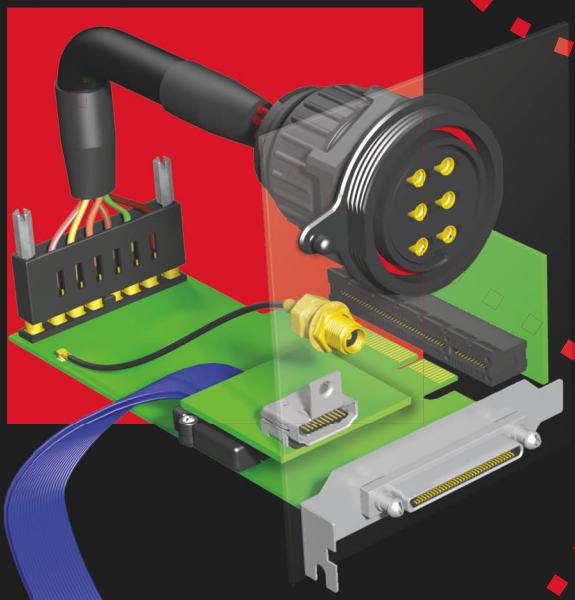
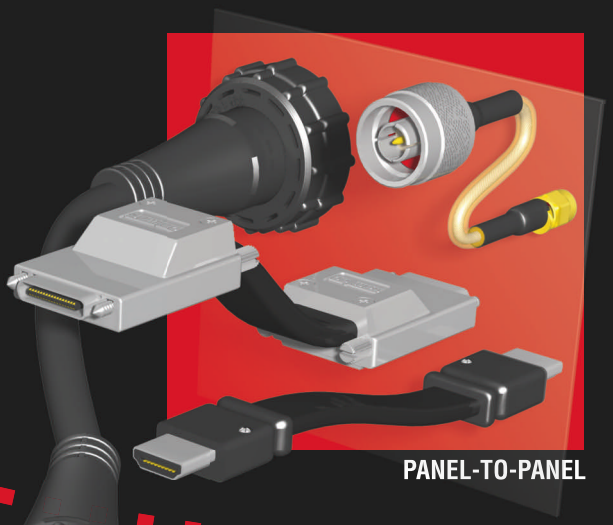
ANALOG DEVICES

# SIGNAL INTEGRITY

PANEL-TO-BOARD

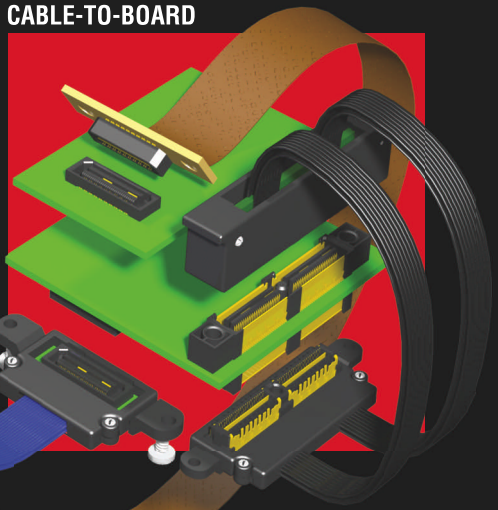


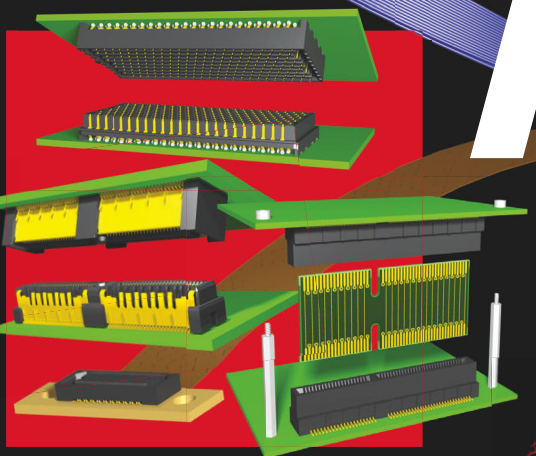


PANEL-TO-PANEL

# FROM THE OUTSIDE IN

CABLE-TO-BOARD





BOARD-TO-BOARD

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EDITED BY FRAN GRANVILLE

# pulse

INNOVATIONS & INNOVATORS

## 7.1-GHz, low-phase-noise spectrum analyzer costs $11,995

Anritsu's MS2717A spectrum analyzer offers general-purpose spectrum analysis over the 100-kHz to 7.1-GHz frequency range at a price of $11,995. Compared with earlier instruments, increased measurement capabilities reduce the cost of and time required for analysis of RF components in wireless, aerospace/defense, and university applications. For characterizing wireless Node B transmitter components, the instrument offers optional WCDMA/HSDPA (wireless-code-division-multiple-access/high-speed-data-packet-access) RF-test and detailed WCDMA-demodulation measurements.

At a cost of $11,995, the MS2717A offers −110 dBc/Hz SSB phase noise and great ease of use for spectrum analysis to 7.1 GHz.

The manufacturer boasts of the unit's low phase-noise: typically, −110 dBc/Hz SSB (single-sideband) phase noise at 10-kHz offsets from carriers at frequencies to 6 GHz. According to the manufacturer, this performance allows the analyzer to easily measure most wireless local oscillators and synthesizers. Typical dynamic range of 100 dB and capture bandwidth of 8 MHz enable fast and precise testing of wireless components that require exceptional linearity. With options, the signal-analyzer-mode frequency ranges are 824 to 894 MHz, 1710 to 2170 MHz, and 2300 to 2700 MHz. An available pass/fail mode based on the five 3GPP (third-generation-project-partnership) test models further simplifies testing.

The 9.53×14.65×13.35-in. instrument, which weighs 12.32 lbs, includes 64 Mbytes of compact-flash memory and provides Ethernet and USB 2.0 connectivity for archiving setups, updating firmware, and transferring results.

**—by Dan Strassberg**

▷**Anritsu Co**, www.anritsu.com.

### FEEDBACK LOOP

**"As always, it is prudent to check your assumptions before you commit your company's human and fiscal resources to a development path. The insight you get might surprise you."**

Mark Jakusovszky in *EDN*'s Feedback Loop at www.edn.com/article/CA6373171. Add your comments.

## Tool generates HDLs directly from Simulink

The folks trying to model multiple DSP functions to implement in FPGAs or ASICs using The MathWorks tools will be happy to learn that the company's latest release, Simulink HDL Coder, automatically generates cycle-accurate, bit-accurate Verilog or VHDL directly from Simulink. Before this announcement, users created Simulink-algorithm-based models of DSPs in Simulink and then had to recode them in VHDL to employ the DSP functions in FPGAs. That step will now be unnecessary, according to Ken Karnofsky, director of marketing for the signal-processing- and communications-products group at The MathWorks.

Sudhir Sharma, HDL-product-marketing manager, says that users can employ the bidirectional tool to both transfer and cosimulate Verilog and VHDL into Simulink models. "You can verify testbenches, intellectual-property blocks, and legacy code in HDL in Simulink, speeding simulation," he says. Because the tool can generate HDL directly from Simulink, you can also run the HDL in FPGAs, representing a big step toward allowing software engineers to directly program designs in FPGAs. Sharma points out, however, that the tool doesn't replace a hardware engineer, because synthesis, routing, and other FPGA-programming functions are still necessary for the FPGA to work properly. Simulink HDL Coder is available for the Windows, Unix, and Linux platforms. The MathWorks offers it in a perpetual license with prices starting at $15,000. Users must also purchase a separate Simulink license.**—by Michael Santarini**

▷**The MathWorks**, www.mathworks.com.

# 55-nm embedded-DRAM process debuts

Many designers think of embedded DRAM—that is, DRAM arrays fabricated on logic SOCs (systems on chips)—as a technological artifact: a technique designers a few years ago tried in moderate-performance graphics chips and since superseded. But NEC Electronics is challenging that opinion with the introduction this month of a 55-nm embedded-DRAM process. An evolution of the company's previously announced, 55-nm, half-step process, this variant may succeed in bringing embedded-DRAM architectures back to center stage in a number of SOC applications beyond just graphics controllers.

The key benefits of the process variant derive from the characteristics of its new DRAM-cell design, according to NEC Senior Design Engineering Manager Hideya Horikawa. The cell uses NEC's MIM (metal-insulator-metal)-2 capacitor structure with zirconium oxide as the high-k capacitor dielectric, the same structure the company uses for its 90-nm processes. But, in the new process, the cell measures 0.12 sq microns—a figure Horikawa believes will be at least 20% smaller than any comparable embedded-DRAM cell. So, in practice, on-chip arrays as large as 4 Mbytes should be feasible.

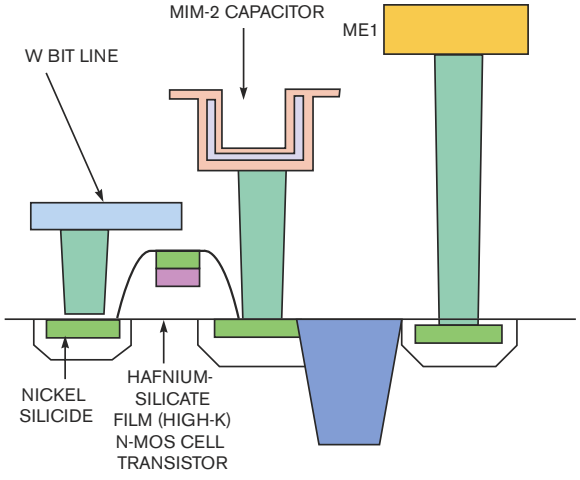
Electrical improvements may be more important than density, however. Horikawa says that the new cell enables 200-MHz cycle rates on full arrays. This feature combines with low operating power to open many new possibilities. The speed and the ability to have wide connections to the array and the flexibility to creatively organize the DRAM macros—in rich multibank schemes, for example—mean that in-system performance of even a large on-chip memory can far exceed what would be possible with external DRAM.

This feature, in turn, suggests that the approach may indeed be useful for applications outside stereotypical embedded-graphics frame buffers. NEC Custom SOC Solutions' vice president and general manager, Kazu Yamada, says that a number of design teams in both the United States and Japan are looking at this generation of embedded DRAM as an addition to the memory hierarchy in nongraphics applications. For example, considerably denser than and with a thousandth the soft-error rate of SRAM but with a speed between that of small SRAM arrays and external DRAM, the structures can act as L2 or L3 caches or as explicitly managed working storage in on-chip multiprocessing systems. This feature can eliminate the headaches of balancing the proliferation of large on-chip SRAM arrays against the complexities of extracting anything approaching theoretical bandwidth from a shared external DRAM.

There is a price to pay: The embedded-DRAM variant adds nine mask steps to the standard 55-nm CMOS process. But—significantly—it does not alter the CMOS-logic structures. So, all intellectual property for the vanilla, 55-nm logic process works with the embedded-DRAM variant, as well. NEC expects to deliver embedded-DRAM macros to design teams by the end of 2006 and to begin production on the 55-nm process in the second half of 2007.

**—by Ron Wilson**

▷**NEC Electronics**, www.necel.com.



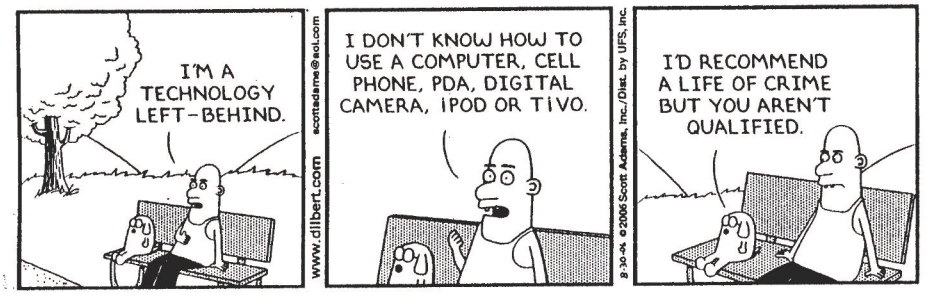

NEC's 55-nm MIM-2 embedded-DRAM cell combines a 0.12-sq-micron area with a 200-MHz system speed.

## FROM THE VAULT

**Will an elite arise if one group of people gains the ability to access information before others, either because they are the developers of the information systems or because they can more easily afford those systems? Will the rich nations get richer and the poor poorer merely because the former possess the resources to develop sophisticated information systems? ... Will society tolerate the condition?**

*EDN*, Oct 14, 1956, pg 39

DILBERT By Scott Adams



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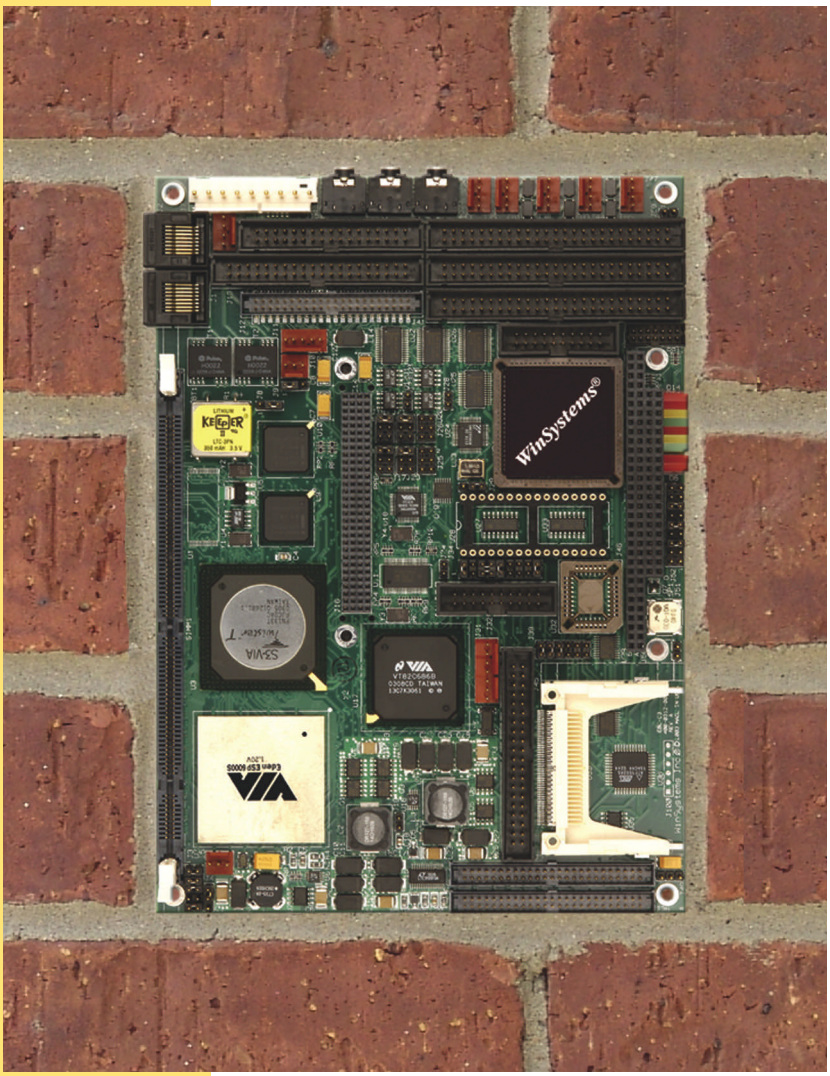


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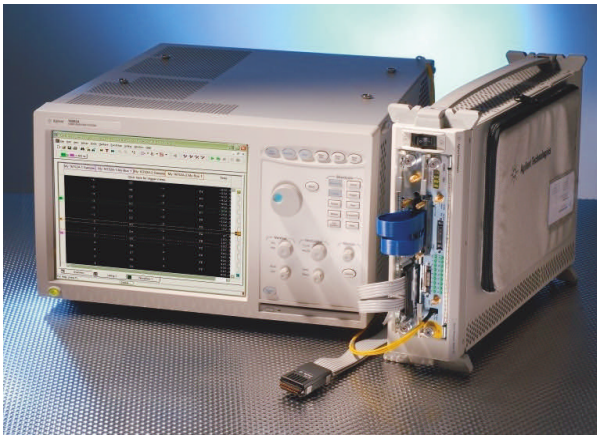
# Test products support PCI Express, HDMI

Agilent Technologies has announced what it calls the industry's first complete and integrated ×1 through ×16 protocol analyzer and exerciser system for 5-Gbps PCIe (PCI Express) 2.0, which doubles the 1.x protocol's speed. The E2960B series addresses the industry's need for a single protocol-test suite that provides nonintrusive measurement of PCIe signals, LTSSM (link-training-and-status-state-machine) testing, and cross-system measurements.

Increasing PCIe's speed to 5 Gbps presents significant challenges to designers of computer and communication systems. The series comprises an analyzer and an exerciser that support both PCIe 1.x and 2.0. Multiple probing options, as well as the newly invented P2L (protocol-to-logic) gateway, complete the system. The analyzer features probes in the midbus 2.0 series that improve upon the current soft-touch midbus probes. The new probes' capacitive loading is less than 0.15 pF; sensitivity is as low as 60 mV.

Before the introduction of the E2960B series, logic and protocol analyzers were separate products. The new series combines key features of both into a single product that enables users to understand data from the physical layer to the transaction layer. Capabilities include the per-lane view, which shows 8-bit/10-bit data even before channel bonding has completed, and the trigger-down-the-lane view, which enables triggering on ordered sets. Per-lane LEDs provide immediate feedback on lane status.



Before the introduction of the E2960B series, logic and protocol analyzers were separate products. The new series combines key features of both into a single product that enables users to understand data from the physical layer to the transaction layer.

In addition, the P2L gateway connects the logic and protocol analyzers, allowing cross-triggering and marker correlation. Connecting multiple instruments and driving them from one station enables broad visibility into the different parts of a system, such as the front-side bus and PCIe, without requiring customers who need only a protocol analyzer to purchase an entire logic analyzer. Prices start at $47,600.

The company also recently announced an updated version of its PCIe electrical-performance-validation and -compliance software, which enables design engineers to test devices to ensure compliance with the PCIe 1.x and 2.0 electrical specifications for add-in cards and motherboard systems. The N5393A software, which runs on Agilent 54855A Infiniium oscilloscopes and 80000-Series oscilloscopes, allows users to automatically execute PCIe electrical-check-list tests and display the results in a flexible HTML-report format. Besides the measurement data, the report provides a margin analysis that shows how closely the tested device passed or failed each test. The list price is $3000.

Agilent also announced an integrated sink, source, and cable-test system for the new HDMI (High-Definition Multimedia Interface) 1.3 standard. The system performs manual and automated HDMI-physical-layer-compliance tests, as well as margin testing and characterization in R&D and manufacturing. Target customers include manufacturers of consumer-electronics products, semiconductor devices, and cables.

Key elements of the new system include Infiniium oscilloscopes; a TDR (time-domain reflectometer); a parallel-BERT (bit-error-ratio tester)-based TMDS (transition-minimized-differential-signaling) signal generator; extensions to the N5590A test-automation software; and HDMI-specific accessories, including the new N1080A-series TPA (test-point-access)-assembly adapters. Point-and-click operations control the integrated system. Compared with previous approaches, the fast calibration time and test throughput increase productivity as much as 50%. Prices start at $165,000, depending on the configuration.

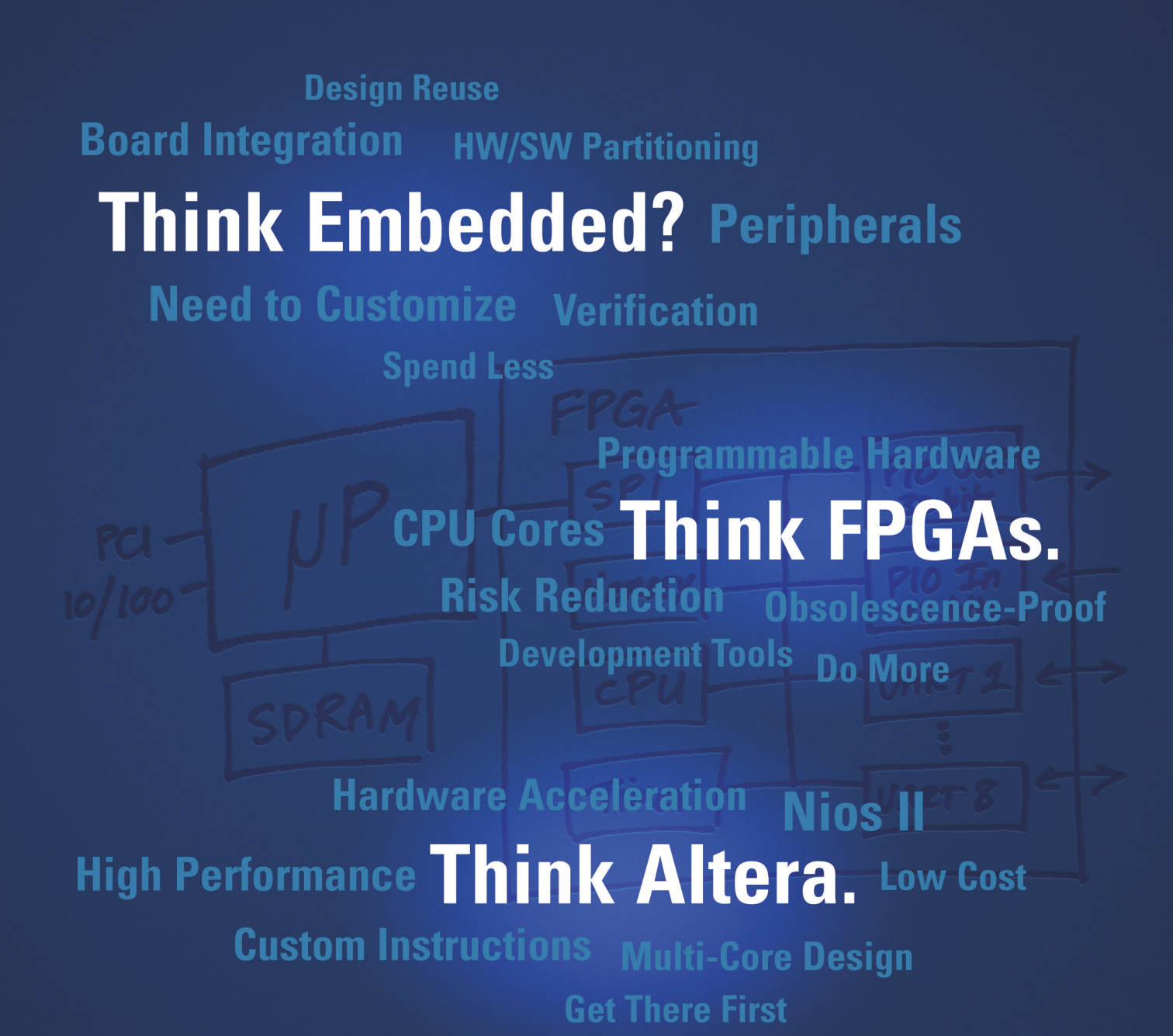
**—by Dan Strassberg**

▷**Agilent Technologies**, www.agilent.com/find/pcie2, www.agilent.com/find/HDMI.

## FEEDBACK LOOP

**"This article not only provides a method by which magnetic coupling can be measured, but also provokes interest in the interference medium, which was for the most part ignored or misunderstood until the associated problems became apparent to the design engineer. Now, he has the opportunity for avoidance and a way to tell how well he has done."**

Bill Singleton in *EDN*'s Feedback Loop, about a recent article on magnetic-field measurements. Read the full article and add your comments at www.edn.com/article/CA6351292.

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# "Lite" version of IP interconnects hardware blocks

While it has been busy licensing its wares into some of the most influential platform designs in the industry, including Texas Instruments' (www.ti.com) OMAP (Open Multimedia Applications Platform) architecture, Sonics has been in an uphill battle to define the concept of interconnect IP (intellectual property). To some engineering minds, interconnect is a physical structure that results from layout and routing. To others, interconnect is a set of architectural decisions. Neither definition fits a traditional notion of IP. To further complicate things, Sonics provides not a core but a development environment, permitting architects to model a block-level-interconnect scheme at a rather abstract level and then nearly automatically move from the high-level model to an RTL (register-transfer-level) implementation. To some engineers, this product seems a lot more like an EDA tool than like an IP core.

The current product, the Sonics MX (multiservice-exchange) interconnect IP, includes a high-level modeling environment. It also includes a set of interface stubs that allows use of either Sonics' own OCP-IP (Open Core Protocol International Partnership) block wrappers or blocks with AMBA (Advanced Microcontroller-Bus Architecture) AXI (Advanced Extensible Interface)- or AMBA AHB (Advanced High-Performance Bus)-compliant interfaces. Additionally, the product features a tool kit of switched and shared-bus fabrics, buffers, and control blocks. The tool set weaves these hardware components into an interconnect structure that ties the user's hardware blocks in a way that meets the performance, power, and quality-of-service requirements that developers design during architectural simulation.

> Chip designers may find that just hooking the blocks together is only the beginning of the problem.

This approach has worked well for the most challenging SOC (system-on-chip) designs, in which both the number of blocks and the interblock-traffic requirements make the design highly complex. But the appeal has been less obvious to less complex designs—those CPU-centric chips with few processors that hover on the boundary between traditional ASICs and SOCs. As these designs get more complex, they start to benefit from the Sonics approach but still can't afford the overhead—either in silicon or dollars—that makes sense on an extremely complex, high-margin chip.

To address what they feel is an emerging market in these less complex chip designs, the Sonics folks have come up with LX (lite exchange), a scaled-back version of MX. Many of the underlying hardware elements are the same, but the LX package offers what Sonics somewhat vaguely calls "a reduced set of design features." The aim is to produce interconnect structures for mid-sized SOCs that are appropriate in both space and power for the smaller problems the tools address but still convenient enough to the design team to justify the expenditure.

This approach may be a hard sell for some teams moving up from simple single-processor ASICs to moderately more complex designs. Such teams have typically developed some facility with AMBA or some other proprietary interconnect architecture and won't see the added value of an interconnect-generating tool. Yet, as these chip designers confront some of the system-level challenges of SOCs, such as optimizing access to a shared DRAM pool, guaranteeing quality of service, providing system-level exception handling, and offering hardware-level security that can meet digital-rights-management requirements, they may find that just hooking the blocks together is only the beginning of the problem. In these cases, an architecture-level interconnect tool capable of RTL generation is indeed worth a look.**—by Ron Wilson**

▷**Sonics Inc**, www.sonicsinc.com.

## DOWNCONVERTER SIMPLIFIES WIDEBAND APPLICATIONS

**Tackling high-performance applications, such as wideband recording, real-time digital-signal processing, software radio, telemetry, and radar-beam forming, Pentek recently released the high-speed, dual-channel Model 6821-422 ADC in a 6U VME form factor. The 6821-422 digitizes the incoming signal at 215 MHz and delivers identical sample streams to two independent digital-down-converter FPGA cores. Within each core, an input stage allows scaling of the ADC samples by a 16-bit gain term.**

**A direct-digital-frequency synthesizer core generates the desired center frequency and delivers two complex local-oscillator signals, offset slightly in phase, to two complex digital mixers that perform frequency translation of the input signal to 0 Hz. The digital output signals are available on two or four front-panel data-port connectors using several data-packing modes. Pentek's C-callable ReadyFlow board-support libraries are available. Prices for the Model 6821-422 module start at $17,495.—by Warren Webb**

▶**Pentek Inc, www.pentek.com.**

The Model 6821-422 preconfigured digital-software-radio subsystem accepts an analog-RF input and delivers real or complex digital-output samples translated to baseband from any frequency slice of the input signal.

10.12.06

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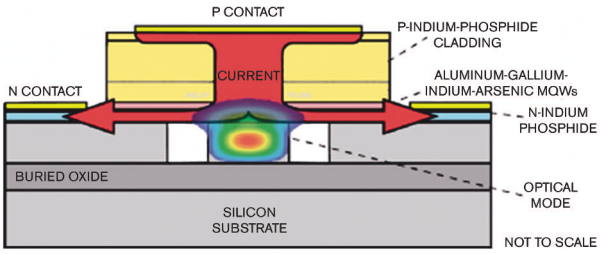
ANALOG DEVICES

RESEARCH UPDATE

BY RON WILSON




Bonding an indium-phosphide layer over a conventional silicon waveguide, Intel and the University of California–Santa Barbara researchers have demonstrated an electrically pumped laser that requires no precision assembly.

## LASER ON A CHIP TARGETS TERABIT RATES

Working with a team at the University of California–Santa Barbara, Intel developers have demonstrated a technique for fabricating very small lasers on the surface of otherwise-conventional silicon ICs without demanding precision alignment or assembly steps. The process could lead to routine use of on-chip lasers for interconnect purposes and, Intel claims, to terabit data rates between chips.

The process starts with the fabrication of a silicon waveguide in an SOI (silicon-on-insulator) wafer. The waveguide has reflective ends to act as a tuned cavity. The researchers bonded a layer of indium phosphide over the entire wafer using low-temperature oxide-bonding techniques. The ability to achieve a strong bond at 300°C is critical, the researchers say, because it makes the step compatible with standard silicon back-end-of-line processing. Finally, the team implants, etches, and contacts the indium-phosphide layer to form an electrically pumped light source directly over the silicon waveguide.

In operation, electrical current higher than approximately 60 mA stimulates photon emission from the indium-phosphide layer. These photons stimulate the tail of a waveguide optical mode that extends up into the interface. This added energy, in turn, stimulates the photon-emission behavior of the silicon, triggering lasing. Researchers have fabricated these devices that operate at 1577 nm at temperatures slightly in excess of 20°C.

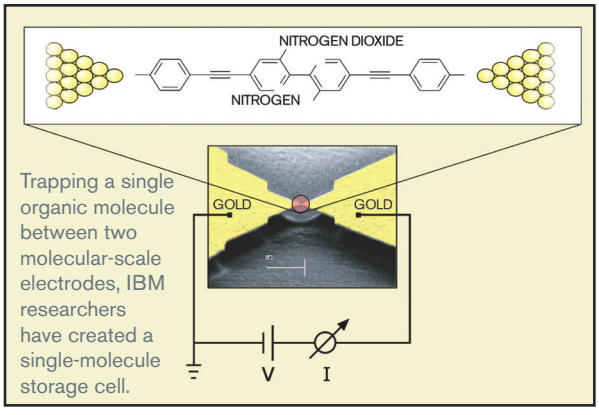
▷**Intel Corp**, www.intel.com.
▷**University of California–Santa Barbara**, www.ucsb.edu.

## 1.5-nm organic cell encapsulates memory

Researchers at IBM's Zurich Research Laboratory have demonstrated a stable, reprogrammable, nondestructive-read-memory effect in a single organic molecule less than 2 nm long. Technicians at Rice University (Houston) custom-designed and synthesized the molecule, BPDN-DT (Bipyridyl-Dinitro Oligophenylene-Ethynylene Dithiol). The Zurich team then devised, in effect, a micromechanical vice to hold the molecule and establish electrical contact with its ends. The team accomplished this goal by fabricating an extremely thin metallic bridge on a flexible insulator and then flexing the insulator until the bridge just tears apart. Researchers then introduce a solution containing the organic molecules and begin to relax the stress. As the two broken fragments of the bridge close together, the desired molecule orients itself between them and becomes fixed.

The Zurich team showed that the molecule exhibited two distinct conductive states and that the team could repeatedly switch between them by applying voltage pulse. The researchers demonstrated endurance of 500 cycles and microsecond-level switching times.

▷**IBM Zurich Research Laboratory**, www.zurich.ibm.com.
▷**Rice University**, www.rice.edu.




Trapping a single organic molecule between two molecular-scale electrodes, IBM researchers have created a single-molecule storage cell.

## Mechanism interlocks nano-oscillators

**Scientists can force the oscillation at microwave frequencies of nanoscale sandwiches in which a layer of copper film separates two layers of magnetic film. However, the resulting devices produce output power on the order of 10 nW–not particularly useful in most applications. They recently discovered, however, that if they placed such nano-oscillators in an array, the devices would phase-lock to each other, and the resulting power output would increase as the square of the number of active devices. However, they did not understand the mechanism for this synchronization.**

**Researchers at NIST, Seagate Research Center, and Hitachi Global Storage Technologies now know why: The oscillators communicate by means of wave patterns that occur in the spins of the electrons in the material between them. The finding is important for its implications in the world of "spintronics," in which researchers encode information into electron-spin patterns instead of into electron-motion patterns.**

▶**National Institute of Standards and Technology, www.nist.gov.**
▶**Seagate Research Center, www.seagate.com.**
▶**Hitachi Global Storage Technologies, www.hgst.com.**

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ANALOG DEVICES

GLOBAL DESIGNER

# Develop software early on virtual ARM hardware

Designers of complex microprocessor-based systems often face the problem of having to develop software before their hardware is ready. According to officials at ARM, that problem becomes particularly acute for developers of high-specification consumer multimedia products. But conventional software-based simulations often run too slowly to be useful. To address the problem, the company has created Realview System Generator, a tool that allows ARM-platform developers tobuild instruction-accurate models that software engineers can use to verify software behavior, because the models run nearly at operating speeds.

The tool operates in a graphical, drag-and-drop style: Users choose blocks from a standard library that includes not only basic ARM-processor elements, but also the company's TrustZone hardware-security and Jazelle Java-acceleration technologies. ARM integrated these tools into the Realview tool flow. Users can debug their models and then use the Realview real-time-system-model graphics-modeling package, which mimics the proposed final form of the product, to test the full user experience with software running. However, the stand-alone-software models do not run within the tool set. They support an operating system with applications running above and still operate at speeds close to those of processors in typical portable products. The model removes as much low-level detail of the hardware implementation as possible and maintains instruction accuracy, ARM says. The company owns the IP (intellectual property) to certify the models as fully accurate.

The speed comes from a translation technology—somewhat similar to a software interpreter—that dynamically translates ARM instructions, block by block, into native instructions for the host processor (Windows and Linux environments on an X86 architecture), holding each block in cache. Peripherals become active only when the system calls them, so the model does not use resources, constantly monitoring their status.

ARM intends that software developers, of whom only a small percentage now use simulation, and professionals creating content in graphics and multimedia-authoring packages use the models. ARM says it will encourage third-party developers within its own product ecosystem to provide models to expand the system; the tool currently supports ARM926EJ-S, ARM1136JF-S, and ARM1176JZF-S cores.

**—by Graham Prophet, *EDN Europe***

▷**ARM**, www.arm.com.

## 3G subscriptions to reach 285 million worldwide by year-end

**After years of market uncertainty, with investors wringing their hands and restructuring their finances, 3G has finally gained credibility, according to ABI Research. Jake Saunders, the company's Asia-Pacific director, says, "3G subscriptions, including CDMA [code-division multiple access] 2000, are forecast to hit 285 million by the end of 2006. Operators' overall capital expenditure will grow for the fourth year to reach $126.4 billion, and annual 3G-related handset shipments should pull past 300 million."**

**W-CDMA (wideband CDMA) is starting to pull its weight in the 3G stakes and is expected to overtake CDMA 2000 by about 2012, but CDMA 2000 is not down for the count: It has proved to be an efficient approach. Nevertheless, W-CDMA will continue to keep the pressure on, and, as end users replace their GSM (Global System for Mobile communications) handsets, many will default to purchasing a W-CDMA handset, providing manufacturers with increasing economies of scale.**

**But not even W-CDMA backers can afford to stand still. TD-SCDMA (time-division-synchronous CDMA) may be taking time to reach commercial reality in China, but Chinese infrastructure vendors, such as Datang Mobile (www.datangmobile.cn/en), are re-engineering their technologies to offer a hybrid TD-SCDMA/HSDPA (high-speed-downlink-packet-access) technology that makes the most of both methods. Don't underestimate WiMax, either. These access technologies dictate the overall cost of service delivery and the functions of the value-added services that operators offer. They also determine which camps of vendors–and their upstream- and downstream-component suppliers–will receive the lion's share of the equipment-spending pie. Intangible factors, such as legacy equipment integration, access to towers, back-haul infrastructure, handset lineups, and vendor financing, also enter the equation.**

**"The exciting prospect is that national markets could be opening up to alternative access technologies more than ever before," says Saunders. "If the vendors of the new alternative 3G+ solutions can demonstrate that they can operate alongside existing 3G and even 2G infrastructures, the opportunities for new entrants or even a few industry veterans, such as Qualcomm (www.qualcomm.com) and Lucent (www.lucent.com) could suddenly look a lot brighter."**

**—by Vinod Kataria, *EDN Asia***

▶**ABI Research,** www.abiresearch.com/home.jsp.

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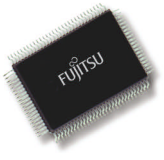


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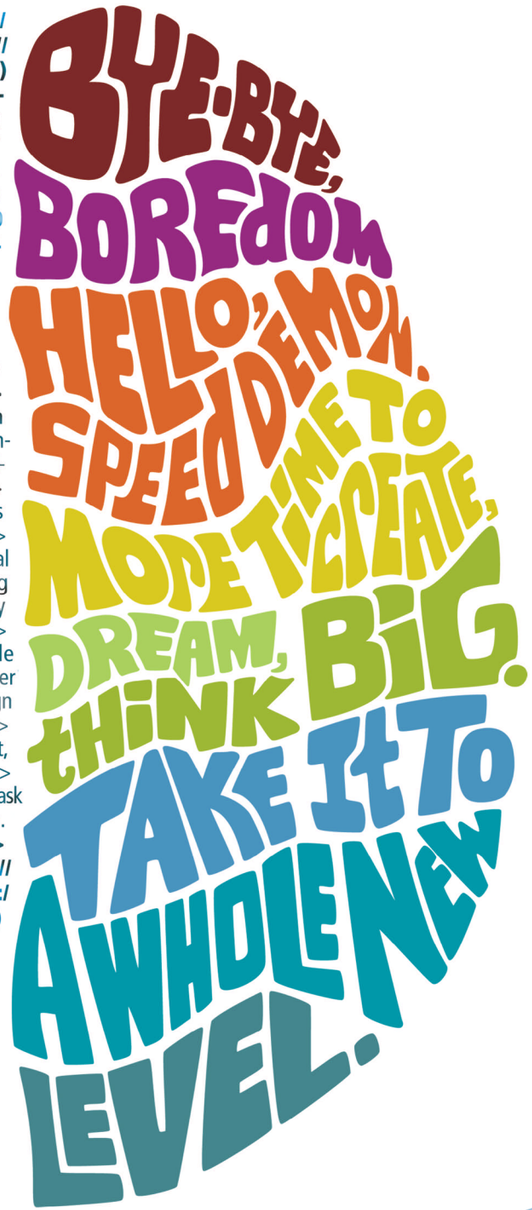


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# Monolithic op amps: A lab tool became indispensable

In the early days, op amps were laboratory curiosities. Based on combinations of discrete tubes and later transistors, op amps formed the basis of analog computers that engineers used to model functions, such as addition or even integration. Some early models even came in wooden boxes. But with the advent of the monolithic op amp in 1963, the device became a hit as a component in system designs.

Robert Widlar of Fairchild (www.fairchildsemi.com) developed the first op amps, the µA702 in 1963 and the µA709 in 1965, before moving on to develop the LM101 at National Semiconductor (www.national.com). In 1968, he wrote a forward-looking-trend article on future op-amp developments as part of *EDN*'s first op-amp directory. You'll find an excerpt of that story below and the complete original article on our Web site at www.edn.com/article/CA6371161.

Over the 38 years since Widlar penned his article, engineers have found every imaginable use for op amps, both as discrete ICs and increasingly as elements in larger IC designs. Within *EDN*'s special 50th-anniversary issue, Analog Devices luminary Lew Counts chronicles the amazing performance gains in op amps over the years and the process-technology advancements that made such improvement possible (see "How miniaturization beats the heat," *EDN*, Sept 28, 2006, pg 174, www.edn.com/060928mini). Counts argues that such analog innovation is equal to Moore's Law in terms of enabling miniaturization.EDN

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FROM THE VAULT

## FUTURE TRENDS IN IC OPERATIONAL AMPLIFIERS

Over the last five years, some outstanding advances have been made in monolithic operational amplifiers. These devices have progressed from the point where they were an expensive curiosity, with marginal performance and doubtful availability, to where their performance is definitely competitive with discrete component amplifiers.

At the same time, prices have dropped, in many cases to a level where it is impossible for discrete-component amplifiers to compete with monolithics in general-purpose applications. Further, multiple-sourcing has become a reality that, in addition to its purchasing advantages, demonstrates that the manufacture of these circuits is not entirely a black art.

The future for monolithic amplifiers indeed looks bright. However, there are many areas in which substantial improvement over present-day devices is needed. Foremost among these are the requirements for lower input currents and higher speed operation. But to gain some insight into the problems of general-purpose op amps, it is advisable to look at all of the parameters that describe their operation, pointing out where improvement is needed and then discussing how it might be done.

Monolithic amplifiers, which inherently have excellent component matching, already provide offset voltages and thermal drifts that are considerably better than discrete amplifiers. In addition, the close thermal coupling among components minimizes the effect of thermal gradients and gives fast recovery from gross overload conditions. Nonetheless, obtaining offsets lower than about 3 mV is a matter of selection, with attendant yield reductions, so great improvements in offset voltage specifications cannot be expected.

It is possible, however, to use adjustable thick-film resistors with the monolithic amplifier to balance out the offset. Techniques are available that use a laser beam to trim the resistors after the complete circuit has been assembled. If this were done, it would be possible to guarantee better drift specifications because the voltage drift could be 100% tested on a go/no-go basis.

Undoubtedly, the strongest factor determining future op-amp designs will be the type of input stage that can give the lowest input current with about the same offset voltage as is currently obtained. At present, integrated op amps using bipolar transistors give input currents of about 100 nA. Many military-temperature-range applications require input currents less than 1 nA, and there are a large number of industrial and instrumentation applications calling for input currents less than 100 pA. Among components now known, the candidates for the input stage are improved bipolar transistors, junction FETs, and MOS FETs.

Perhaps the most straightforward way to get low input currents is to use junction field-effect transistors in the input stage. With discrete devices, input currents in the picoampere range can be realized over a 0 to 70°C temperature range. One disadvantage of FETs is that they do not tend to match well.

Even so, one can expect to see monolithic amplifiers with FET inputs within the next six months. These will give considerably improved input current specifications over the industrial temperature range, but at the expense of offset voltage and offset voltage drift. The success of these devices will depend heavily on elimination of production difficulties and on achievement of reasonable yields since industrial-range devices sell solely on cost.

—by RJ Widlar, *EDN*, June 10, 1968

ANALOG edge℠

Expert tips, tricks, and techniques for analog designs

Vol. IV, Issue 10

DESIGN idea

# Amplifier Closed-Loop Bandwidth Considerations in High Resolution A/D Converter Applications

*By Jerry Freeman, Applications Engineer*

## Amplifier Bandwidth Limitations

Amplifier closed-loop bandwidth-limited accuracy considerations are critical when driving high resolution A/D Converters (ADCs). It is useful to be able to predict, for any closed loop gain, the required gain-bandwidth (GBW) product of an op amp to achieve a specified level of accuracy in terms of the minimum ADC resolution. Other sources of error include offset, noise, and distortion, which are beyond the scope of this article. A simple equation will be developed below that relates the minimum closed-loop bandwidth of an op amp to the resolution requirements of a given ADC.

## Amplifier Response

Assuming a single pole roll-off, the frequency dependence of an amplifier's closed-loop gain, $A_{CL}$, is given by:

$$A_{CL} = \frac{A_{CLDC}}{\sqrt{1+\left(\frac{f}{f_{-3\,dB}}\right)^2}} \qquad \textit{Equation 1}$$

where $A_{CLDC}$ is the amplifier's DC gain, and $f_{-3\,dB}$ is its corner frequency.

This equation describes the op amp's closed-loop gain at frequency ***f***, in terms of the amplifier's corner frequency.

The vast majority of op amps employ internal lag compensation with a single dominant pole that rolls off the open-loop gain, from its cut-off frequency, to unity gain (zero dB) at a 20 dB per decade rate. The frequency response of such an amplifier with feedback is therefore also the same as for an RC low-pass filter. The frequency where the open-loop gain crosses unity gain is routinely called the GBW product in op amp datasheets. The GBW product for an amplifier is the product of its open loop gain (constant for a given amplifier)

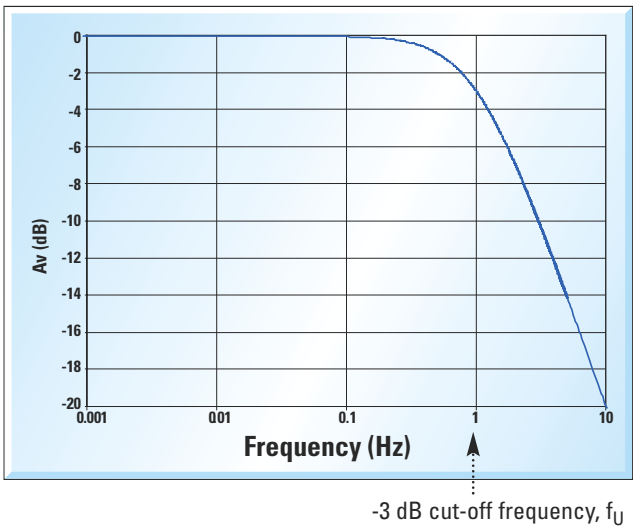


**Figure 1. Normalized bandwidth curve for an op amp in unity gain (Curve assumes an open loop gain with a single pole roll-off.)**

and its -3 dB bandwidth (GBW product = gain x -3 dB bandwidth). Given the GBW product and the open-loop gain roll-off of -20 dB per decade, the -3 dB bandwidth for any closed loop gain can be easily calculated, from

$$BW = GBW / A_{CL} \qquad \textit{Equation 2}$$

For example, the LMP2011 with a GBW product of 3 MHz will have a bandwidth of 300 kHz when configured with an $A_{CL}$ of 10 V/V. However, at -3 dB the closed-loop gain has a 29.3% gain error. In reality, the gain expression starts rolling off long before the -3 dB pole frequency is reached. It is important to determine the frequency at which the closed-loop gain error increases above the maximum error allowed for a given data error. The maximum error in data

**NEXT ISSUE:**

**Dithered Switching Frequency**

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The extended temperature range of -40°C to 125°C allows for operation in demanding industrial and automotive applications, as well as in precision instrumentation amplifiers, thermocouple amplifiers, and strain gauge bridge amplifiers. The LMP2011 is offered in SOIC-8 and SOT23-5 packaging. The LMP2012 is offered in SOIC-8 and mini SOIC-8 packaging. The LMP2014 is offered in TSSOP-14 packaging.

For FREE samples, datasheets, and more, visit
**www.national.com/pf/LM/LMP2011.html**
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  - +0.06, -0.05 LSB (ADC081S051)
- Differential Non-Linearity (DNL):
  - +0.5, -0.25 LSB (ADC121S051)
  - +0.15, -0.11 LSB (ADC101S051
  - +0.06, -0.045 LSB (ADC081S051)
- Signal-to-Noise Ratio (SNR):
  - 72.0 dB (ADC121S051)
  - 61.6 dB (ADC101S051)
  - 49.6 dB (ADC081S051)

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# Amplifier Closed-Loop Bandwidth Considerations in High Resolution A/D Converter Applications

converters is usually expressed in terms of the Least Significant Bit (LSB). Ideally, all error sources should be well below this level. An LSB of an ADC is defined as the finest resolution of which the ADC is capable. Quantitatively this is equal to the full scale voltage divided by the resolution of the ADC ($V_{FS}/2^N$) for one LSB, were N is the number of bits. Thus for an 8-bit converter, the error would be $V_{FS}/256$. If $^1/_2$ LSB is set as the required system accuracy, the acceptable accuracy limit would be:

**Accuracy (δ) = 100% - gain error (%),**

where gain error = 1/2 ($1/2^N$) *100%, *Equation 3*

which gives **δ = 100% - 1/2 ($1/2^N$) *100%,** or 99.8%

The accuracy is calculated based on the -3 dB cut-off frequency at a particular close-loop gain. Approximating the frequency response of an op amp to that of a single pole filter, we get the frequency vs gain curve of such a system as shown in ***Figure 1.***

Because the curve is normalized to 1 for a frequency $f_U$ (-3 dB at unity gain), the expression for this curve, for any ***f***, from ***Equation 1*** is

$$A_{CL} = \frac{1}{\sqrt{1+(f)^2}} \qquad \textit{Equation 4}$$

Solving for f gives

$$f = \sqrt{\frac{1}{(A_{CL})^2} - 1} \qquad \textit{Equation 5}$$

The question is now, for any ACL, what is the maximum signal frequency that does not exceed the specified error? From ***Equation 1, Equation 3,*** and ***Equation 5***, and the example for 8-bit accuracy, the normalized frequency, $f_{MAX}$, for an amplifier requiring 99.8% accuracy, is the frequency where the gain roll off is less than $^1/_2$ LSB is expressed as

$$f_{max} = \sqrt{\frac{1}{(0.998)^2} - 1} \times f_U = 0.062 \times f_U \qquad \textit{Equation 6}$$

for the case of unity gain.

Thus, the maximum frequency at which it is still possible to get at least 99.8% ($^1/_2$ LSB) accuracy in an 8-bit system, is 0.062 of the op amp's -3 dB frequency. In the case of the LMP2011 example, the available bandwidth for 99.8% accuracy is

$$0.062 \times f_{-3\,dB}\ \text{kHz} = 0.062 \times 300\ \text{kHz} = 18.6\ \text{kHz}$$

In general, the normalized $f_{MAX}$ for $^1/_2$ LSB error for ADCs of various resolutions can be calculated as

$$\text{Normalized } f_{MAX} = \sqrt{\frac{1}{\left(1-\frac{1}{2^{n+1}}\right)^2} - 1} \qquad \textit{Equation 7}$$

Using this equation, a list of normalized bandwidths for system resolutions up to 16 bits have been calculated *(Table 1)*.

| System Resolution | Normalized Bandwidth for <1/2 LSB Error |
|---|---|
| 8-bit | 0.062592 |
| 9-bit | 0.044227 |
| 10-bit | 0.031261 |
| 11-bit | 0.022101 |
| 12-bit | 0.015626 |
| 13-bit | 0.011049 |
| 14-bit | 0.007813 |
| 15-bit | 0.005524 |
| 16-bit | 0.003906 |

**Table 1. Calculated maximum frequency with an error less than $^1/_2$ LSB at the specified resolution**

## Conclusion

Obtaining dynamic performance compatibility between an amplifier and an ADC in data acquisition designs requires careful analysis of the amplifier's bandwidth capability. Choosing an amplifier that satisfies the bandwidth requirements of the system on the basis of its GBW product specification can introduce an excessive amount of error into the system. The amplifier must be chosen such that its closed-loop bandwidth matches the resolution needs of the ADC. This dictates the need for a much wider bandwidth amplifier than would be suggested by the specified signal bandwidth in the amplifier's datasheet. ■

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  - +0.3, -0.2 LSB (ADC101S101
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### Features

- ±150 µV (max) input offset voltage
- 100 fA input bias current
- 5.8 nV/$\sqrt{\text{Hz}}$ input voltage noise
- 17 MHz gain bandwidth product
- 1.15 mA supply current (LMP7711)
- 1.30 mA supply current (LMP7712)
- 0.001% THD+N at f = 1 kHz
- Rail-to-rail output swing

Operating at -40°C to +125°C, these precision amplifiers are ideal for use in sensor interface applications, transimpedance amplifiers, and active filters and buffers. The LMP7711 is offered in Thin SOT23-6 packaging and the LMP7712 is offered in a MSOP-10 packaging.

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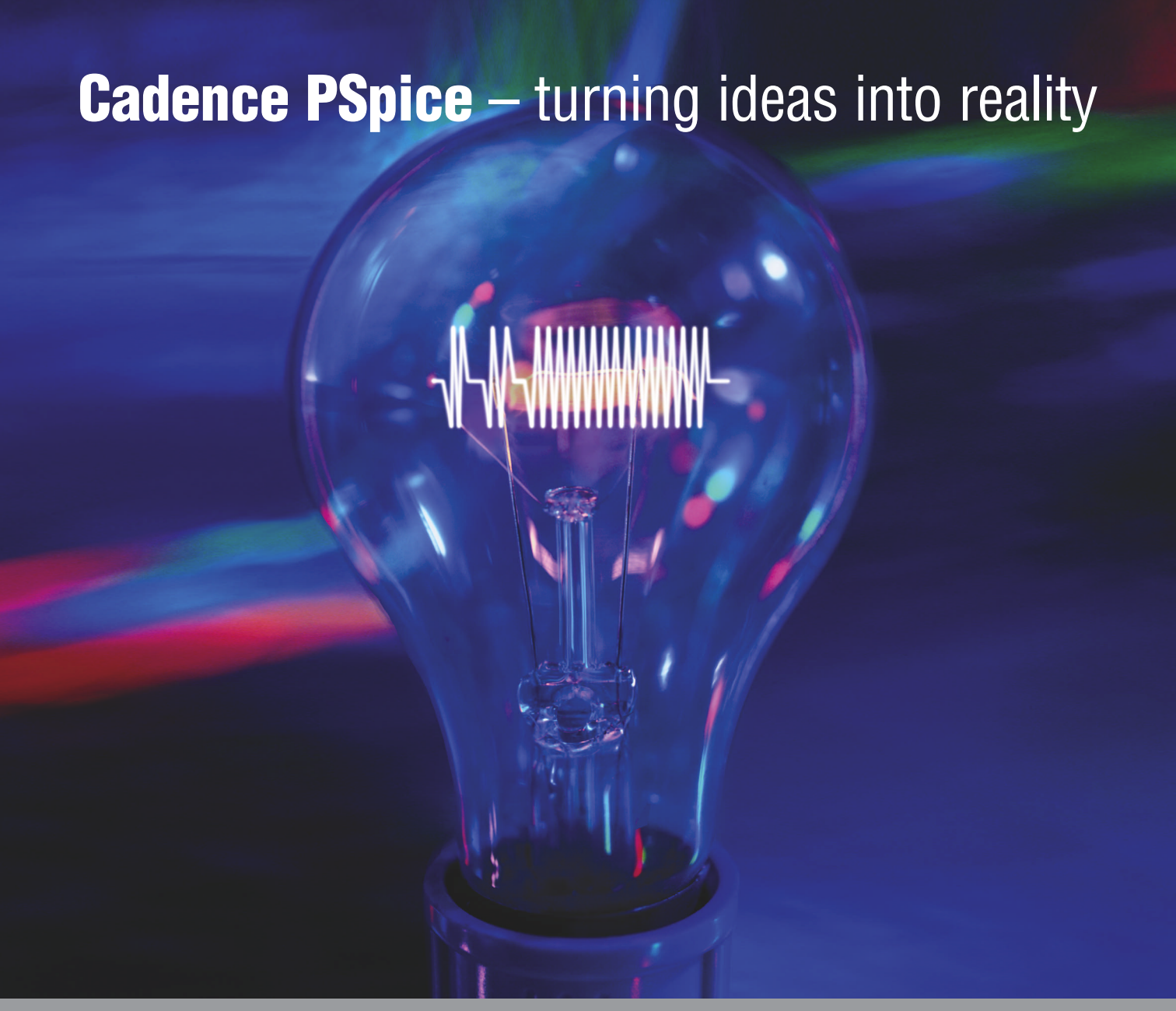

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BY HOWARD JOHNSON, PhD

# Frequent obsession

I recently encountered yet another pc-board-trace specification written in the frequency domain. Why do people do that?

This particular specification calls for a worst-case trace loss of −3 dB at 11.2 GHz. The trace goes inside a piece of test equipment that works at 3.2 Gbps.

The specified frequency, 11.2 GHz, is *much higher* than the system data rate. You may infer from the specification that the system designer wants an *extremely* clean channel with rise and fall times far shorter than the data-bit interval.

Unfortunately, the specification may *imply* a clean channel, but it doesn't *specify* one. All it says is "worst-case trace loss of −3 dB at 11.2 GHz."

A number of systems that meet this overly stringent specification fail to deliver good performance at 3.2 Gbps.

For example, a 10th-order, Butterworth brick-wall lowpass filter with a −3-dB cutoff residing precisely at 11.2 GHz satisfies the specification to a tee, but its time-domain response rings prodigiously.

Similarly, a poorly terminated transmission line with hideous overshoot could still meet the letter of the specification, but probably not your idea of a "clean channel."

The ambiguity in this specification derives partly from its frequency-based orientation and partly from its lack of detail.

To address the lack of detail, you could add more frequency points to the specification; stipulate both magnitude and phase information; and call for a smooth, monotonic frequency response. These additions make a more impressive-sounding specification but fail to directly address your main concern: time-domain performance.

**No time-domain instrument can surpass the accuracy, sensitivity, noise floor, and autocalibration routines inherent to a network analyzer.**

To control the time-domain shape of signals conveyed through any linear, time-invariant system, you should specify a time-domain test. My preferred arrangement is a step-response test. The test should call out four main points:

- The amplitude, rise time, and source impedance of the required step source.
- The method of connection to the system. Always provide test connectors for this purpose.
- The test load (50Ω, or 100Ω differential, in most cases).
- A template for the received step.

A good template specifies the required minimum and maximum rise time and may also require a monotonic step response or otherwise limit the size and number of ripples.

Make sure the template depicts the signal shape resulting from excitation with your practical test source, not just the raw "idealized" step response of the system given a perfect step input.

Frequency-domain instruments can play an important role in the measurement process but should not be the main focus of your specification.

For example, if you have a vector-network analyzer and you know how to use it, you can measure the S-parameter response of your system. Then use the FFT (Fast Fourier Transform) to compute the time-domain step response of your system. Measure that time-domain result against your template.

I like this hybrid approach because no time-domain instrument can surpass the accuracy, sensitivity, noise floor, and autocalibration routines inherent to a network analyzer. If you use a network analyzer, do it to gain these advantages, not because you have become, like too many engineers lately, simply obsessed with the frequency domain.

Time matters.EDN

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*Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.*

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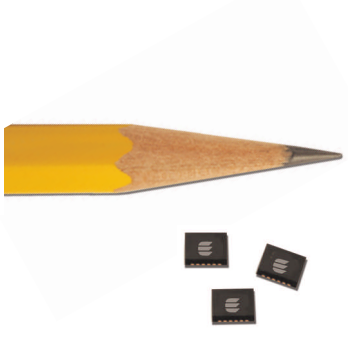

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JAMES LONG, PHD

# Sidebands be gone, or let there be (no) light

DANIEL VASCONCELLOS

Back in 1983, I was working at ESL (Electromagnetic Systems Labs) in Sunnyvale, CA, on exotic, high-performance radios. I had done all the calculations and developed a circuit for one of these radios. The prototypes had come in, and I was pleased with much of the design. There was one problem, though: spurious sidebands on the synthesizer output. I feared that I had created some type of sensitive node in the synthesizer and that power-line ac hum was polluting the RF signal.

Fortunately, ESL had a "screen room"—a gaussian chamber enclosed in small-gauge-copper-mesh screening. The size of the mesh prevents any external signals from penetrating into the space. I took the synthesizer prototype and the spectrum analyzer into the chamber. The 120-cycle sidebands were still in the synthesizer output. I thought the problem was the receiver's power supply, so I tried running the synthesizer from a battery. You can't get much more dc than that.

After trying that tack, the sidebands were still there! I was going crazy. However, while repositioning a piece of lab equipment above the bench, I noticed out of the corner of my eye that the sideband level was changing. I waved my arms above the receiver. The sidebands disappeared as my arms passed over the chassis. I wondered whether I had created a theremin. (A theremin is a musical instrument consisting of an array of circuitry, including two antennas around which the user moves his hands; it requires no physical contact to produce music.)

Instead, though, I realized that several glass-encapsulated, variable-capacitance diodes were in the VCO (voltage-controlled oscillator). As a result, it was picking up the 120 Hz in the varying intensity of the fluorescent lights above the bench. I placed a black-velvet cloth that I found in the lab over the prototype: no sidebands. Then I tried turning off the lights: still no sidebands.

What really annoyed me is that I knew clear-glass-encapsulated variable-capacitance diodes would cause sidebands. Even with that knowledge, however, I never suspected that they had in fact caused the sidebands because they were painted black—mostly. What I did not notice is that the ends of the diode bodies, right where the leads went in, were unpainted. Eureka! These clear, unpainted ends were allowing the light in. (Despite this cautionary tale, be aware that, with modern electronic-fluorescent ballasts, you might see effects at other frequencies besides 120 Hz.)

To this day, a mystery still remains unsolved: Where did the black-velvet cloth come from? Such items are not common in an electronics laboratory. EDN

*James Long, PhD, is an analog and RF consultant in Sunnyvale, CA. He holds an extra class ham-radio license and received his first license in 1963.*

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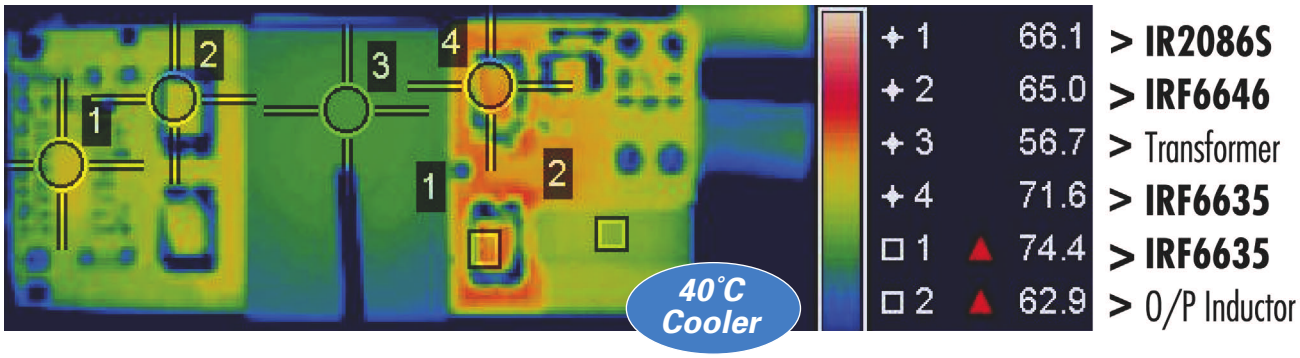


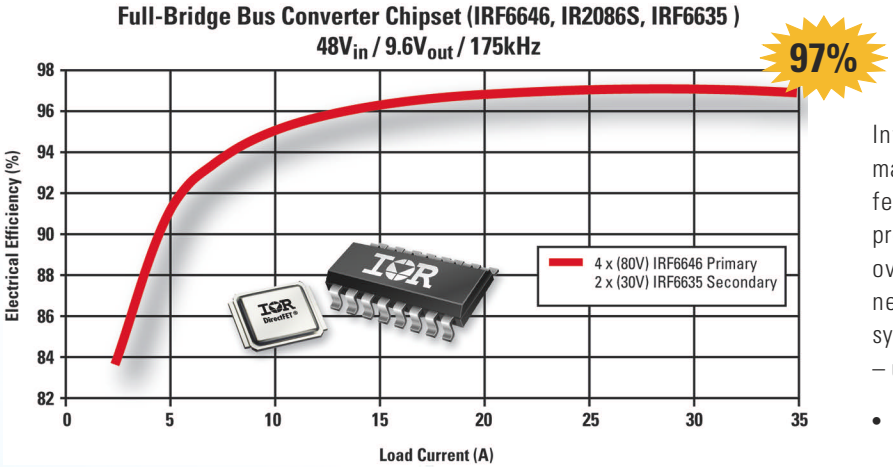


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| IRF6655 | Small can | 100V | 62mΩ | 8.7nC | 2.8nC |
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| IRF6638 | Medium can | 30V | 2.9mΩ | 30nC | 11nC |
| IRF6635 | Medium can | 30V | 1.8mΩ | 47nC | 17nC |
| IRF6631 | Small can | 30V | 7.8mΩ | 12nC | 4.4nC |
| IRF6629 | Medium can | 25V | 2.1mΩ | 34nC | 11nC |
| IRF6628 | Medium can | 25V | 2.5mΩ | 31nC | 12nC |
| IRF6622 | Small can | 25V | 6.3mΩ | 11nC | 3.8nC |

| Control IC | | | |
|---|---|---|---|
| Part # | Package | Voltage Rating | Description |
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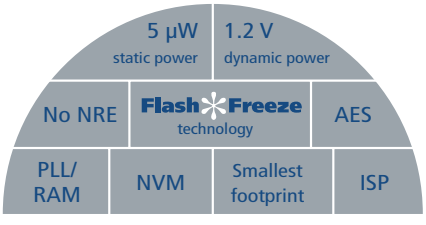


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CONSUMERS WANT PAINLESS NETWORKING AND INTEROPERABILITY OF MULTIMEDIA DEVICES. HERE, TWO STANDARDS GROUPS PAINT SOMETIMES-CONFLICTING PICTURES OF HOW TO ACHIEVE THAT GOAL—AND HOW FAR SUCH SHARING SHOULD EXTEND.

# DLNA and HANA: two visions of consumer multimedia networking

We're a long way from the idealistic vision of mobile gadgets, living-room entertainment systems, and home PCs all sharing multimedia without a hitch. Indeed, today's digital consumer devices tend to be idiosyncratic, isolated, and unwilling to share their audio and video treasures.

Two industry groups, the DLNA (Digital Living Network Alliance, www.dlna.org) and the HANA (High-Definition Audio-Video Network Alliance, www.hanaalliance.org), are working on open standards that they claim will provide the "seamless" interoperability that consumers—thanks to premature hype—now believe to be imminent. The groups' visions share common elements and even overlap in many respects. But on some issues they disagree vehemently.

If you're working in the consumer realm, you may soon have to grapple with which of these standards to support, not to mention when and how to do so. *EDN* invited representatives from each group to lay out the scope of their plans, detail their progress, and make their case to the engineering community.

## DLNA: EMBRACE THE ENTIRE ECOSYSTEM

***Scott Smyers, DLNA***

The DLNA, now in its fourth year of operation, is aggressively and successfully addressing the issue of interoperability among devices in the consumer's digital-AV universe. Although the alliance has a broad and ambitious scope and goal—encompassing consumer-electronics devices, PCs, and mobile devices such as portable video players and multimedia cell phones—the DLNA is making unmistakable and unprecedented progress, as is evident by a growing slate of DLNA-certified products in the marketplace.

The DLNA targets a consumer-

focused ecosystem of interoperable products that allows access to and enjoyment of content in a substantially better way than today's confusing and inconsistent home-networked world. The organization is working to provide consumers with seamless and convenient access to all forms of content in a manner that is transparent, that protects the consumer's investment in commercial content, that protects the rights of content owners, and that respects the consumer's sensibilities and expectations of access and usability. These goals are collectively consistent and synergistic. With its progress toward these goals, the DLNA is enabling the next killer app: easy access to content, anywhere, at any time, and on any authorized device in the consumer's interoperable domain.

Through its efforts, the DLNA's goal is to bake a bigger pie from which all participants can take a rightful piece. This goal stands in contrast to current examples of individual companies that are working to make a pie that they wholly control. It also stands in contrast to recent industry activities that hoped to create interconnected technology islands that stood in isolation, before it became clear that connectivity to the global Internet would become a business necessity, as it now has.

To be clear, the DLNA is working to create a thriving, sustainable ecosystem that is an integral part of the Internet, and, to this end, the DLNA's technology platform is founded on proven and ubiquitous Internet protocols. The DLNA ecosystem includes device manufacturers, service operators, retailers, and content owners. And it is an open ecosystem, in which all parties can participate and from which all parties can derive business value.

## STACK DEFINED

To achieve its admittedly ambitious goals, the DLNA must establish an actual, adequate, and usable platform without going too far up the stack and without falling short of the goals. History provides a long list of efforts with scopes too narrow—or too broad—to be commercially useful.

The DLNA has carefully chosen its target for the overall interoperability stack. At the lowest level of that stack, the DLNA has established 802.11a, b, and g, plus wired Ethernet. Although the DLNA guidelines spell out these physical interfaces, other physical interfaces can carry the DLNA stack, provided that they have IP (Internet Protocol) mapped onto them. Future DLNA guidelines may include other physical interfaces, depending on the interests and support of DLNA members.

THE ORGANIZATION SEEKS TO ENSURE THAT DLNA-CERTIFIED DEVICES WILL MEET EXPECTATIONS WHEN THE CONSUMER DISCOVERS SOME INTERESTING PIECE OF CONTENT AND HITS THE VIRTUAL "PLAY" BUTTON.

Moving up the stack, the DLNA has chosen the UPnP (Universal Plug-n-Play) Device Architecture, or UDA, Version 1.0. The UDA provides network autoconfiguration, device discovery, and device capabilities and service discovery. Next, the DLNA guidelines document how to use the UPnP CDS (Content Directory Service) for content discovery and selection. Above that, the DLNA guidelines identify HTTP (Hypertext Transfer Protocol) for device communication and content movement across the network.

On top of this stack is the DLNA media-format-interoperability model. This model identifies a set of media formats that are necessary to achieve interoperability. Each format in the set of required formats is an open standard, and the DLNA bylaws themselves legislate this restriction. This step ensures that open industry standards will provide the foundation of media-format interoperability for all time.

In addition to the required media formats, the DLNA has published a set of optional media formats. Manufacturers of DLNA-compliant devices are free to implement and use any documented optional format, provided that it enables them to interoperate successfully. In the event that two devices do not implement the same optional format, they must then use one of the required formats to achieve interoperability.

This scenario means, for example, that a DLNA-compliant server must transcode content from an optional format into one of the required formats in the event that the server is attempting to stream content to a player or a rendering device that implements only one of the required formats or one that implements a different optional format. Using this mechanism, the organization seeks to ensure that DLNA-certified devices will meet expectations when the consumer discovers some interesting piece of content and hits the virtual "play" button.

This DLNA stack provides a solid foundation for interoperability. Content of all types, including commercial content, will flow across that foundation. To protect commercial content, the DLNA has now finalized its Link Protection Guidelines, which the organization will publish in the near future. These guidelines rely on well-known and trusted content-protection technologies to meet first-stage, near-term content-protection requirements.

The DLNA has recently chartered a new subcommittee to continue work on commercial-content interoperability. In setting up this work, the DLNA leadership expended great effort to set directions and realistic, but commercially useful, goals. The first fruits of this effort are the aforementioned Link Protection Guidelines. The DLNA based the next goal on the realistic expectation that at any point in history, more than one DRM (digital-rights-management) system will be operating in the world of consumer devices.

Choosing and mandating a single DRM system for all devices, therefore, are unrealistic goals, and achieving these goals is not the DLNA's intention. Instead, the DLNA is seeking technology approaches that address what the

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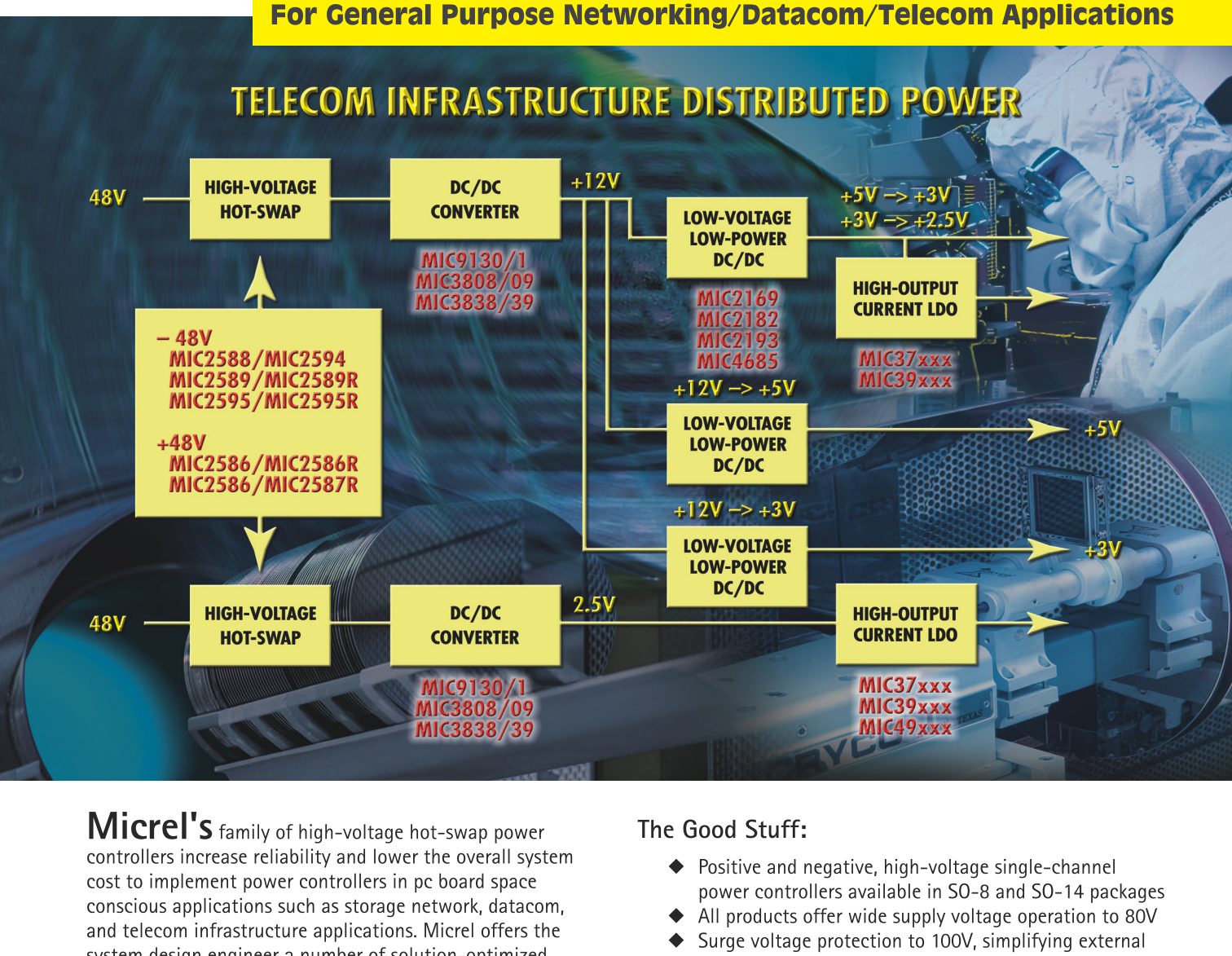


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organization calls DRM interoperability. "DRM interoperability" means that, even if you own a variety of content that an array of DRM technologies protects and even if you own a variety of devices that collectively implement a multitude of DRM technologies, you should be able to access all content that you are authorized to access on all legitimate devices that you own. This goal is another ambitious one, to be sure, but one that is at hand, thanks to the realization, among all participants in the consumer-product and commercial-content value chains, that network interoperability is the foundation for the next killer app.

## UNPRECEDENTED EFFORT

In its short existence, the DLNA has realized a rock-solid platform of interoperability based on proven, ubiquitous, and open industry standards; a certification and logo program that speaks to the consumer; and an effective process for building on the interoperability platform and managing the evolution of technology. These achievements represent a degree of collaboration we've never before witnessed in any standards-setting body. Moreover, DLNA has chosen the right target, going as far up the stack as necessary to realize interoperability without going too far up the stack or limiting member companies' ability to differentiate.

DLNA has earned the interest and participation of content owners and service operators, thereby ensuring that commercial content will flow and that the DLNA platform will support the deployment of new services and content businesses. Device retailers are also actively participating in DLNA efforts to bring the interoperable home network to the consumer. In short, DLNA is delivering on its promise, and the future is bright.


## AUTHOR'S BIOGRAPHY

*Scott Smyers is the chairman of the DLNA. He is also the vice president of the Network and Systems Architecture Division of the Platform Technology Center of America at Sony Electronics (www.sony.com).*


# HANA: FIRST, FIX THE LIVING ROOM

***By Bill Rose, WJR Consulting***

Years ago, all you had to do to watch TV was connect one wire and pick up one remote. Modern AV systems deliver a far richer experience, of course, but they have also become so complex that consumers have difficulty installing and even using them. HANA wants to restore the simplicity of that earlier era and still allow consumers to enjoy all of the latest capabilities.

HANA has developed a standards-based framework that delivers interoperability among home-entertainment devices and also simplifies setup. The cornerstones of this approach include requiring only one connection cable for each device and allowing a single remote to control multiple devices through simple on-screen interfaces.

Because DLNA is also promoting a standards-based approach to interoperability, it's fair to ask whether both are necessary. You could argue that, because DLNA is addressing every kind of network-enabled device, including home-entertainment equipment, PCs, and mobile devices, HANA is redundant. However, HANA's members believe that DLNA, by attempting to address everything over a single network based on PC-networking concepts, risks exporting PC-like complexity to the family room. Everything will indeed be connected. But will watching TV get easier or more difficult than it is today?

HANA and DLNA both address Layer 3 (the IP layer) and above, meaning that they do not explicitly specify physical and MAC (media-access-control) layers. However, both groups have made some assumptions about the underlying network technology based on their needs and the world from which they evolved. DLNA assumes that Wi-Fi, Ethernet, and USB will carry both content and control information. HANA, recognizing that the network must be invisible to the user, has focused initially on IEEE 1394, also known as FireWire.

## WHY 1394?

IEEE 1394 provides both isochronous transport of AV content and asynchronous delivery of data. It also offers other services that asynchronous, best-effort networks, such as Ethernet and Wi-Fi, lack. These services include automatic device discovery, a systemwide clock to synchronize audio and video content (for lip-synching and multiroom audio applications), and guaranteed QOS (quality of service) using bandwidth reservation.

Ethernet and Wi-Fi require additional protocol layers and therefore complexity to even begin to approach these capabilities. This scenario is fine in PCs and other devices that have ample memory to buffer content, processing horsepower to execute complex software stacks, and the ability to accept upgrades in the field. But AV products lack these luxuries. So, HANA's approach dictates that any entertainment device should contain everything it will ever need the day the manufacturer ships it from the factory. It should be able to connect to future products—in one year or in five years—without software upgrades. And, most important, it must be absolutely reliable: no hiccups, no blue screens, no rebooting.

HANA achieves these goals by letting every device send its user interface, including control menus, play lists, and other information, to the display. The TV does not need to know much about the connected device; it simply displays the information it receives and lets the user make selections. Want to watch a movie stored on your DVR? Select the DVR as the source and you will see its play list. Select the program and hit "play." Want to finish watching it in the bedroom? Simply pause the program, go to the bedroom, select the DVR, and hit play again.

What happens in the background to support this scenario? When a user plugs a 1394 device into the network, every connected device immediately and automatically receives notification that a new device has joined. That notifica-

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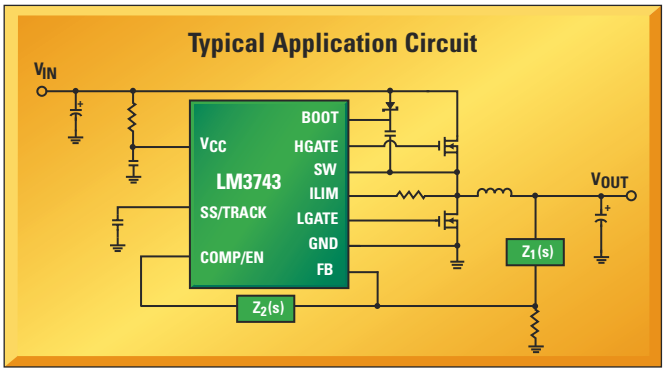


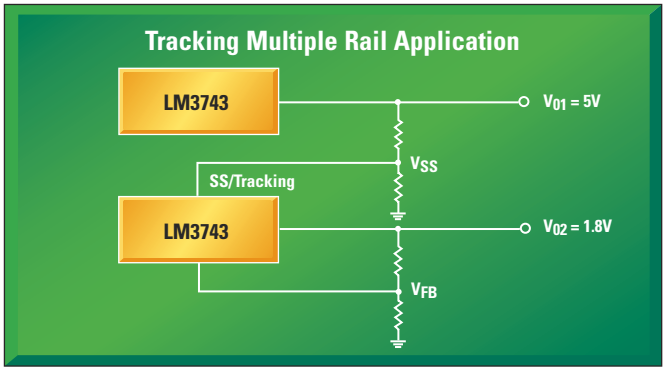


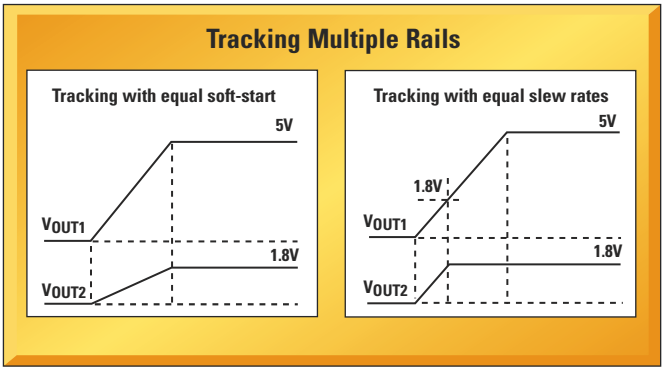


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tion describes the new device and the types of commands it supports. These steps all happen at the 1394 layer. Next, the device obtains an IP address using standard IP discovery. Thereafter, the systems employ Internet protocols such as HTTP, xHTML, and others for command and control and to establish and dissolve logical connections between devices. However, whereas DLNA specifies HTTP as the transport protocol, HANA uses isochronous transport as defined in IEEE 1394/61883, which guarantees low-latency delivery of content using bandwidth reservation.

When a consumer selects a device, such as a DVR, a browser in the TV reads a predefined URL in the DVR, which then serves up a Web page containing its top-level menu for the TV to display. The consumer selects the desired function using the TV's remote control, and the TV sends that selection to the DVR, which executes it. The TV does not need to know what the action is. If the user chooses to play a movie, for example, the DVR simply establishes the isochronous connection with the TV and starts streaming the movie. If an action involves multiple devices—such as changing a set-top box to a given channel at a specific time and recording that program on a DVR—one of the devices, which the HANA design guidelines define, acts as the coordinator and orchestrates the activity.

HANA also defines proxies that allow non-HANA devices to participate on a HANA network. For example, if a user plugs in a legacy FireWire camcorder that is unable to serve up its own menu, the TV will display a generic user interface with standard playback and recording functions.

Meanwhile, a HANA-DLNA gateway will provide the necessary proxy between UPnP, which DLNA uses, and HANA, enabling rich interaction between devices. Critically, such a gateway will also isolate traffic that does not need to, or should not, travel between the two networks. This feature is important not only because the QOS capabilities of 1394 far exceed those of asynchronous networks, but also because commercial content may carry restrictions on its use.

Finally, HANA is working with cable companies and the 1394 Trade Association to enable high-definition cable set-top boxes to connect using the 1394 ports they already have, thanks to an FCC (Federal Communications Commission) mandate, but are not using (see sidebar "The case of the unused 1394 ports").

## FIRST THINGS FIRST

HANA sees the work of the DLNA and the UPnP Forum as crucial if we are to get to a point where everything connects to everything else in and beyond the home. However, HANA members and many others believe that, at least initially, it is more important to simplify the entertainment experience than it is to connect more things to the entertainment system.

HANA is neither about networking, 1394 or otherwise, nor about any particular physical medium. It is about letting everyone enjoy high-definition entertainment, anywhere in the home, anytime they want, without having to read instruction manuals or employ their own IT departments. The network is simply a means to an end. And, if Ethernet, Wi-Fi, USB, HomePlug, HomePNA (Home Phoneline Networking Alliance), MoCA (Multimedia over Coax Alliance), or some other technology can provide the connections with the necessary reliability and simplicity, HANA will embrace them, as well. EDN

## THE CASE OF THE UNUSED 1394 PORTS

**Thanks to an FCC (Federal Communications Commission) mandate, all high-definition cable set-top boxes include a 1394 port. However, most of these ports remain unused.**

**There are two reasons for this situation. First, cable set-top boxes render a rich GUI (graphical user interface), which they then send in uncompressed form to the TV in one of three ways: over DVI (Digital Visual Interface), over HDMI (High-Definition Multimedia Interface), or as an analog signal. No current home-networking technology, including Gigabit Ethernet, can cost-effectively support uncompressed high-definition signals.**

**The second reason that cable companies have ignored the 1394 port is that they do not install Category 5 or 6 UTP (unshielded-twisted-pair) wire. They pull coaxial cable. Faced with the choice of training thousands of installers to install thousands of miles of UTP cable in homes or placing a set-top box at each TV, they have opted for distributed set-top boxes.**

**The HANA (High-Definition Audio-Video Network Alliance) is working with member companies and cable companies to enable the networking of an OCAP (OpenCable Application Platform) GUI over 1394. And the 1394 Trade Association, in partnership with HANA member companies, is developing 1394 over coaxial cable at 400 Mbps. These developments will allow cable companies to finally employ those 1394 ports. And, from the consumer perspective, these changes would allow a single set-top box to drive displays throughout a home.**


## AUTHOR'S BIOGRAPHY

*Bill Rose, president of WJR Consulting, is also the chairman of the Consumer Electronics Association's R7 Home-Networking Committee. He participates in all of HANA's technical and business working groups and task groups and leads the technical working group.*


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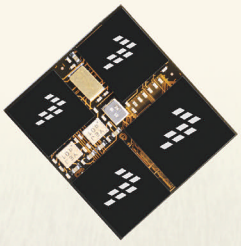

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# PCI EXPRESS CONTENDS FOR COMMUNICATIONS ROLE

SCALABLE PERFORMANCE AND LOW COST ARE MAKING PCI EXPRESS ATTRACTIVE FOR COMMUNICATIONS-DEVICE DESIGNS, CHALLENGING PROPRIETARY-BUS STRUCTURES FOR NEXT-GENERATION DESIGN WINS.

Replacing PCI as a peripheral bus in general-purpose computers, PCIe (PCI Express) is now seeking a role in communications. It offers the raw performance for communications and has significant cost advantages over today's popular proprietary buses. Its legacy link to the PC may limit its communications success, however, unless proponents can solve critical shortfalls in its architecture.

Decades after it surfaced, the IBM PC is still having a ripple effect throughout the electronics industry. The PC's immense popularity and resulting production volumes have made PC-centric technology both inexpensive and widespread. These advantages, in turn, have made the technology appealing to a variety of other applications. The PC's bus structures have spun off a number of derivatives, including PC/104, PXI, and CompactPCI, which make the PC's processor, peripheral devices, and software elements available to non-PC applications.

PCIe is the most recent version of the PC's peripheral-bus structure to begin finding its way into other applications. As with the earlier PCI and AT buses, PCIe is generating interest because it allows embedded-computing developers to use the proven, powerful, low-cost, and widely available technology that arises from desktop computing. Unlike the previous buses, however, PCIe offers performance levels that match the processor's—with room to grow. At the same time, PCIe retains software compatibility with the PCI bus, preserving the cost advantages that previous generations of PC technology have enjoyed (see **sidebar** "PCI Express basics").

This combination of high performance and low cost has caught the attention of the communications industry. Traditionally, communication developers have used proprietary-bus structures to handle their highest performance needs. Cost and time-to-market pressures, however, have made proprietary approaches increasingly unattractive.

Still, the home that PCIe will find in the communications market is not yet certain. Communications devices have a broad range of needs, varying with their position in the network hierarchy. This hierarchy spans multiple levels with differing mixes of control and data-handling requirements (**Figure 1**).

## VARYING NEEDS

The transport tier lies at the high-data-rate end. This tier provides long-distance data transport over high-capacity channels. Statically configured transport-tier devices do not interact significantly with the data they are transporting. As a result, these devices are not strong candidates for PCIe. Devices start to become aware of the data they handle at the core tier, although their interaction with the data is still limited. Core devices prioritize their functions based on the tags and labels added to the data in the lower tiers. Typically, core devices use an architecture that separates the control of the data from the handling of the data. The control plane manages the tables that direct the data plane in routing the data through the system. Whereas PCIe may have a role in the control plane of core-tier devices, the data plane tends to employ proprietary-bus structures and protocols to minimize the packet-routing overhead and achieve high bandwidth efficiency.

### AT A GLANCE

- PCIe (PCI Express) replaces the PC's parallel PCI bus with a switched serial bus that offers software compatibility.
- The cost and availability of such PC hardware make it attractive to other applications.
- The scalable bandwidth performance of PCIe gives it the raw performance to match many communications-system requirements.
- PCIe allows only a single master processor, making it awkward for implementing redundancy and high-availability design.

High-end edge-tier devices often have similar architectures to but lower performance demands and greater data interaction than core devices. These tier devices provide service-aware QOS (quality-of-service) enforcement and traffic management. Lower end edge devices are typically aggregation nodes that help maintain a relatively even amount of traffic to and from the high-end edge devices to maximize edge bandwidth-usage efficiency. At this tier, the performance of PCIe begins to more clearly match the needs of both control and data planes.

The strongest match, however, occurs at the access tier, at which users connect to the network through a service provider. At this tier, requirements are diverse because the access tier must handle a variety of protocols, including data, voice, and multimedia, in its interaction with the end user. In addition, physical considerations, such as the distance to the user, affect the requirements. Designs for this equipment show considerable diversity in their number of ports, node capacity, and redundancy strategies. Designers can choose from multiple architecture options, including separated control and data planes and merged traffic, in these designs.

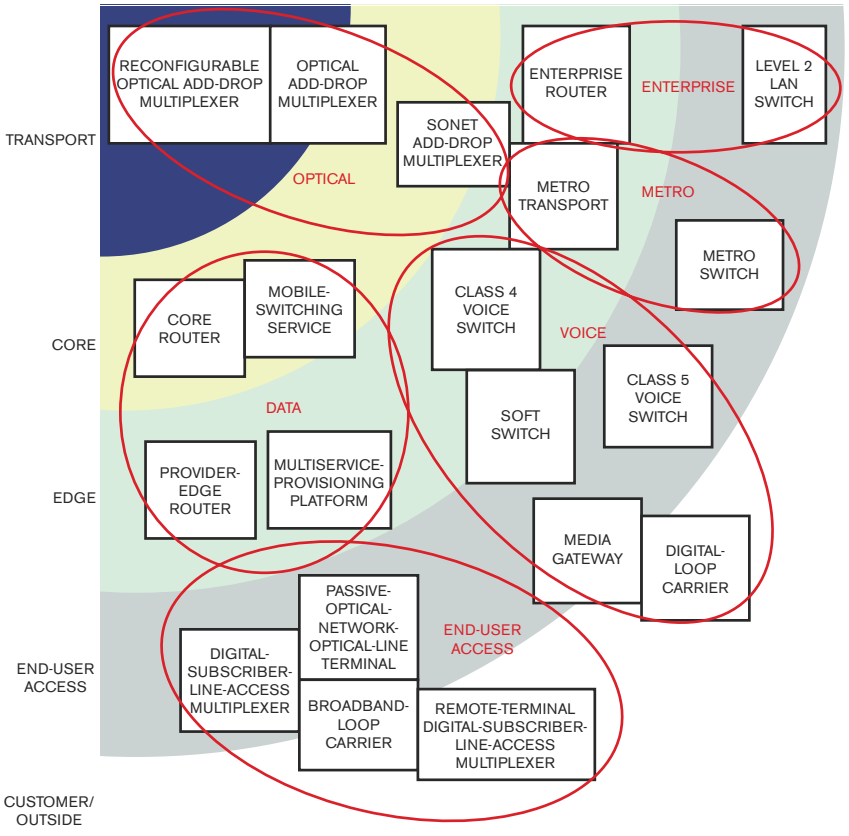
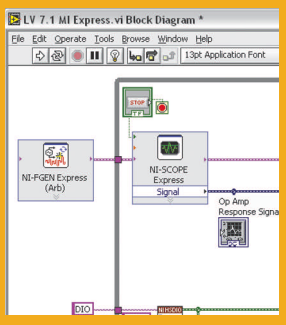
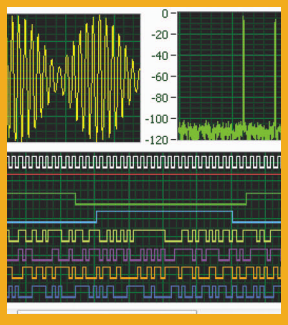
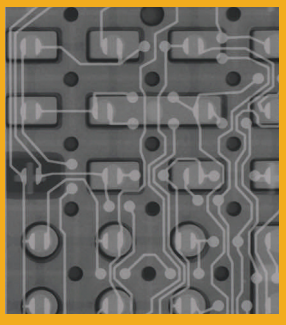
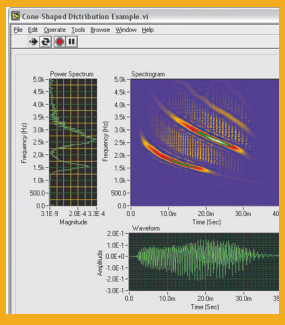


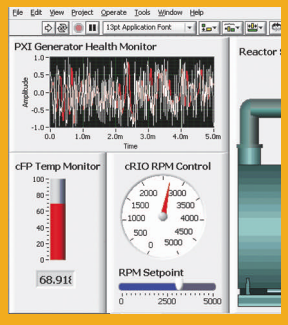

Figure 1 Devices for the communications market, depending on the tier in which they operate, vary in their bus needs and the applicability of PCI Express (courtesy IDT).

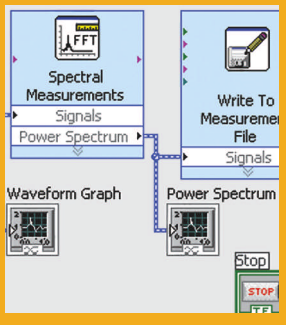







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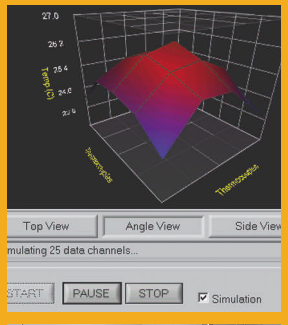



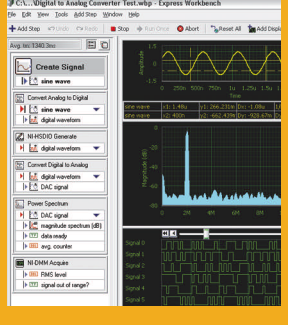

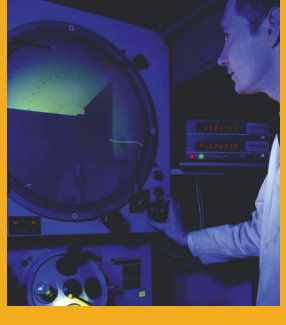
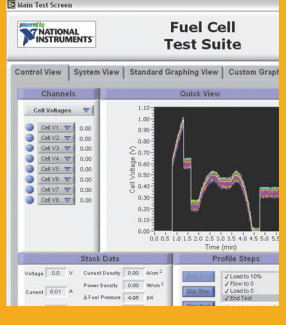


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# PCI EXPRESS BASICS

Parallel buses become harder to implement as clock speeds increase and skew between clock and signal lines becomes an ever-larger percentage of the clock cycle. As a result, the PCI bus has languished at a modest clock rate of 266 MHz while processor clock speeds have topped 1 GHz. To eliminate this mismatch and the system bottleneck it causes, the PCI-SIG (PCI Special Interest Group) developed PCIe (PCI Express). The group's goal was to bypass the bandwidth limitations of a parallel bus and maintain application-software compatibility with PCI.

A PCIe bus comprises a set of parallel "lanes" that make a point-to-point connection between two nodes, such as the CPU and a peripheral controller. A multiport switch at the center of a star topology allows the point-to-point PCIe connections to replicate the many possible paths of a traditional parallel bus (Figure A). With the appropriate design, the switch can also allow two or more paths to operate concurrently as long as they do not share the same ports.

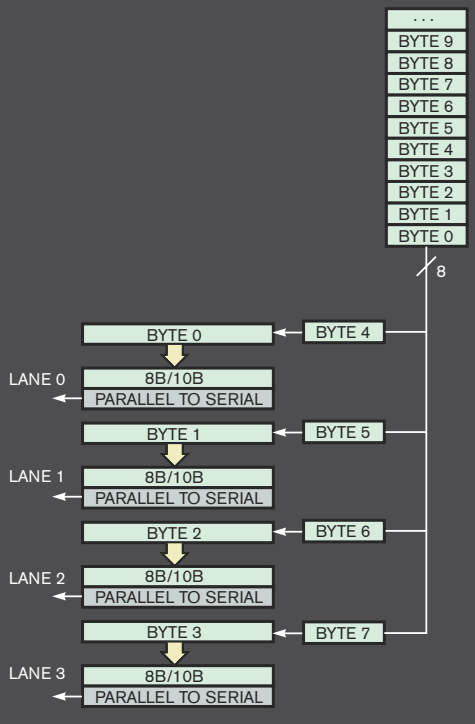



Figure A Physical-layer hardware in PCI Express automatically stripes successive data bytes across whatever lanes are available and recombines them in the proper order at the receiving end.

The lanes in PCIe are serial links that operate with 8b/10b encoding at a 2.5-GHz clock rate. Each lane has a forward and a return channel and uses differential signaling for a total of four wires per lane. To provide for bandwidth scaling, PCIe allows the connection between nodes to comprise one, two, four, eight, 12, 16, or 32 lanes. A PCIe connection can thus offer a raw data rate ranging from 250 Mbytes/sec to 8 Gbytes/sec. A pending upgrade to the PCIe specification will increase the allowable serial clock rate to 5 GHz, doubling the bandwidth capacity of a given lane configuration.

Designs need not use devices with matched lane counts. During power-up initialization or following a plug-and-play board insertion, nodes negotiate the lane width of the connections they will use. Thus, a device with a 16-lane interface can communicate at its full bandwidth with 16- and 32-lane devices and at decreasing bandwidths with devices having fewer lanes.

Maintaining application-software compatibility with the parallel PCI bus while operating over a variable-width serial bus requires several modifications at the lower levels of the communications model. At the physical layer, for instance, a PCIe link includes hardware that stripes data bytes across the available lanes for transmitting and reassembles them at the receiving end. The serial-data packets contain header information that allows the reassembly of packets in the correct order even if they arrive at different times, eliminating the effects of skew between lanes.

The link layer handles the detection of and response to transmission errors in the serial links. Each packet sent to the physical layer includes a packet sequence number and a CRC (cyclic-redundancy-check) character for error detection. If a transmission error occurs, the link-layer hardware automatically resends the damaged packets.

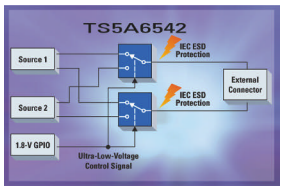
The transaction layer interacts with the system software to convert a software agent's memory-mapped read and write transactions that target the PCI bus into command and data packets that pass to the PCIe link layer. Each packet includes a unique identifier that associates it with a given transaction. This identifier allows the layers to route the outgoing transmission to the appropriate node and to route responses to the appropriate software agent.

The transaction layer supports memory, I/O, and configuration spaces within the system and can handle both 32-bit and extended 64-bit addressing. These capabilities make PCIe able to fully mimic the load-store architecture and flat memory space of a PCI bus, so none of the higher software levels in the system need alteration. Applications, operating systems, and hardware drivers developed for PCI all work unaltered with PCIe hardware.

In addition to the memory-mapped transactions over the parallel bus, the PCI bus includes sideband signals, such as interrupts, power management, and reset. PCIe handles these functions by incorporating them into a message space. The PCIe-interface hardware converts such sideband signals into data packets that run over the serial links along with the command and data transactions. The sideband signals are reinterpreted as control lines at the node. Thus, PCIe provides "virtual wires" to replace the interrupts and other control lines of PCI.

The structure of PCIe does more than simply mimic the PCI bus to legacy software, however. It also offers new features that new software can exploit. One such feature is the ability to assign attributes such as "relaxed-ordering" or "priority" to packets. The system can use these attributes when managing the switch and resolving contention between nodes for I/O resources. Thus, PCIe can support the QOS (quality-of-service) features that communications applications such as VOIP (voice over Internet Protocol) require.

# Analog Switches from Texas Instruments



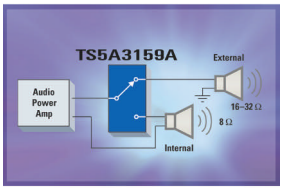

▶ **Single SPDT analog switch with input logic translation and IEC ESD (TS5A6542)**

– +/- 15kV IEC 61000-4-2 Contact Discharge ESD protection (common pin)

– Low ON-state resistance (0.75Ω max)

– Excellent ON-state resistance matching

– Break-before-make switching



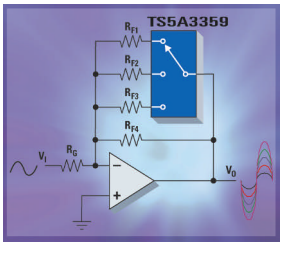

▶ **Single 0.9-Ω SPDT analog switch (TS5A3159A)**

– 100-MHz bandwidth – highest of any 3159-type in the industry

– Ultra-small wafer chip scale packaging

– Wide low-voltage operating range: 1.65 V to 5.5 V

– Break-before-make switching




▶ **Single, 0.9-Ω SP3T analog switch (TS5A3359)**

– Space-saving integration eliminates the need for using serial connected SPDT analog switches

– Isolation in the powered down mode (V+ = 0V)

– 1.65-V to 5.5-V single-supply operation (Control Inputs are 5.5 V tolerant)

– Break-before-make switching

| Device | $r_{on}$* (Ω) (max) | $r_{on}$ Flatness (Ω) (max) | $r_{on}$ Mismatch (Ω) (max) | $V_+$ (V) (min) | $V_+$ (V) (max) | ON Time (ns) (max) | OFF Time (ns) (max) | Pins/Packages |
|---|---|---|---|---|---|---|---|---|
| **SPST** | | | | | | | | |
| TS5A3166 | 0.9 | 0.15 | — | 1.65 | 5.5 | 7 | 11.5 | 5/SC70, SOT-23, WCSP |
| TS5A3167 | 0.9 | 0.15 | — | 1.65 | 5.5 | 7 | 11.5 | 5/SC70, SOT-23, WCSP |
| TS5A4594 | 8 | 1.5 | — | 2.7 | 5.51 | 7 | 14 | 5/SC70, SOT-23 |
| TS5A4595 | 8 | 1.5 | — | 2.7 | 5.51 | 7 | 14 | 5/SC70, SOT-23 |
| TS5A4596 | 8 | 1.5 | — | 2.7 | 5.5 | 17 | 14 | 5/SC70, SOT-23 |
| TS5A4597 | 8 | 1.5 | — | 2.7 | 5.5 | 17 | 14 | 5/SC70, SOT-23 |
| TS5A1066 | 10 | 5 | — | 1.65 | 5.5 | 5.5 | 4.5 | 5/SC70, SOT-23, WCSP |
| **SPST x 2** | | | | | | | | |
| TS5A23166 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 7.5 | 11 | 8/US8, WCSP |
| TS5A23167 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 7.5 | 11 | 8/US8, WCSP |
| **TS3A4741** | 0.9 | 0.4 | 0.05 | 1.65 | 3.6 | 14 | 9 | 8/SSOP, MSOP |
| TS5A2066 | 10 | 5 | 1 | 1.65 | 5.5 | 5.8 | 3.6 | 8/SM8, US8, WCSP |
| **SPST x 4** | | | | | | | | |
| **TS3A4751** | 0.9 | 0.4 | 0.05 | 1.65 | 3.6 | 14 | 9 | 14/TSSOP |
| **SPDT** | | | | | | | | |
| **TS5A6542** | 0.75 | 0.25 | 0.25 | 2.25 | 5.5 | 25 | 20 | 8/WCSP |
| TS5A4624 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 22 | 8 | 6/SC70 |
| TS5A3153 | 0.9 | 0.15 | 0.1 | 1.65 | 5.5 | 16 | 15 | 8/US8, WCSP |
| TS5A3154 | 0.9 | 0.15 | 0.1 | 1.65 | 5.5 | 8 | 12.5 | 8/US8, WCSP |
| TS5A3159A | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 30 | 20 | 6/SC70, SOT-23, WCSP |
| TS5A3159 | 1.1 | 0.15 | 0.1 | 1.65 | 5.5 | 35 | 20 | 6/SC70, SOT-23 |
| TS5A3160 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 6 | 13 | 6/SC70, SOT-23 |
| TS5A3157 | 10 | 5 | 0.2 | 1.65 | 5.5 | 8.5 | 6.5 | 6/SC70, SOT-23, WCSP |
| TS5A63157 | 10 | 2 | 0.14 | 1.65 | 5.5 | 5 | 3.4 | 6/SC70, SOT-23 |
| TS5A2053 | 13.8 | 4.5 | 4.5 | 1.65 | 5.5 | 6.8 | 4.1 | 8/SM8, US8 |
| **SPDT x 2** | | | | | | | | |
| **TS5A23159** | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 13 | 8 | 10/MSOP, QFN |
| TS5A23160 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 5.5 | 10 | 10/MSOP |
| TS5A23157 | 10 | 4(typ) | 0.15(typ) | 1.65 | 5.5 | 5.7 | 3.8 | 10/MSOP |
| **SPDT x 4** | | | | | | | | |
| TS3A5018 | 10 | 7 | 0.8 | 1.65 | 3.6 | 8 | 6.5 | 16/SOIC, SSOP (QSOP), TSSOP, TVSOP,QFN |
| **SP3T** | | | | | | | | |
| **TS5A3359** | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 21 | 10.5 | 8/US8 |
| TS5A3357 | 15 | 6.5(typ) | 0.1(typ) | 1.65 | 5.5 | 6.5 | 3.7 | 8/SM8, US8 |
| **SP4T x 2** | | | | | | | | |
| TS3A5017 | 12 | 9 | 2 | 2.3 | 3.6 | 9.5 | 3.5 | 16/SOIC, SSOP (QSOP), TSSOP, TVSOP, QFN |

**Data measured under typical conditions with maximum $V_+$.*
*Data collected as of 7/06*

*New Products are listed in **bold red**.*

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With separate control and data planes, a communications device has two sets of bus requirements. The control plane handles access to control registers and counters and the movement of data blocks into and from table memory. This situation means that the bus traffic typically flows between a central housekeeping CPU and individual data-handling nodes. This type of traffic is a good match with the memory-mapped-addressing structure that PCIe inherited from the PC architecture. As a result, PCIe is a strong candidate for the use of control-plane buses within communications devices. Similarly, PCIe matches the needs of merged control and data planes. Its high performance supports the necessary data rates, and the structure maps well to the need of the control plane to access the data headers before initiating data movement.

The data plane has a different set of requirements, however. Its primary need is to move data at high speed from any input port to any output port that the device provides. A traditional multidrop parallel bus, such as PCI, is inefficient at meeting this need. Although multidrop buses allow cross-connectivity, only one pair of devices can communicate at a time. PCIe, however, uses switches in its datapaths. These switches can be nonblocking—that is, able to connect multiple pairs of ports at the same time (**Figure 2**). This ability means that PCIe potentially offers a suitable data-flow structure for handling data-plane requirements. PCIe fares less well with some other architectural requirements of data planes, however. One of the most significant is the need for redundancy.

## THERE CAN BE ONLY ONE

Communications systems, particularly at the higher tiers, need extremely high reliability. The complete failure of a node can bring the network to a halt. At best, a node failure represents lost revenue and a set of angry customers. As a result, communications systems require redundant designs that allow multiple CPUs to operate concurrently.

PCIe allows only a single point of control. In a PC, the central processor initializes and controls all other elements in the system, forming a single system

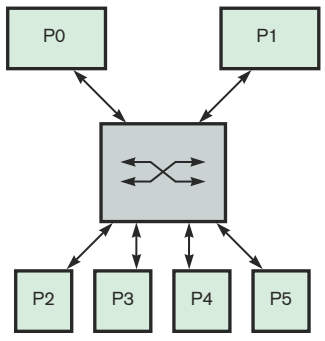


Figure 2 Switches in PCI Express, configured as two-by-eight lanes (top) or four-by-four lanes (bottom), connect pairs of ports together and, if nonblocking, can support two or more simultaneous connections, such as P1 to P3 and P2 to P5, as long as there is no port contention (courtesy NEC).

complex. It does not provide for multiple independent processors to have access to resources within the complex. If one of the other system elements is also a processor, that second processor must be a slave to the central processor; it cannot initiate any transactions to peripheral devices on its own. Similarly, PCIe does not support having multiple processor complexes share access to system resources.

Recognizing this limitation in PCIe, the PCI-SIG (PCI Special Interest Group) that governs the PCIe standard is actively working on a solution. Its approach, IOV (I/O virtualization), allows multiple processors and processor complexes to share peripherals and other system endpoints. The virtualization will be available at two levels. The peripheral or endpoint itself provides the first level: single-root virtualization. At this level, the endpoint provides its resources, including interrupts and direct-memory access, independently to each processor. In second-level IOV, the endpoint and the switch have mechanisms that allow multiple processor complexes to share a common endpoint resource.

IOV is still under development, however. Developers seeking to add system redundancy within the current PCIe specifications can choose one of two approaches. One is to use multiplexers that connect the primary- and the backup-system elements to the PCIe switches in a dual-star topology (**Figure 3**). The other approach is to use a nontransparent switch, such as those from IDT, Intel, and PLX Technology.

## MULTIPROCESSING NEEDS

A nontransparent switch takes packets coming from a processor complex on one side and converts the addressing elements in the header to map the packets to the processor complex on the other side. During power-up, a PCIe

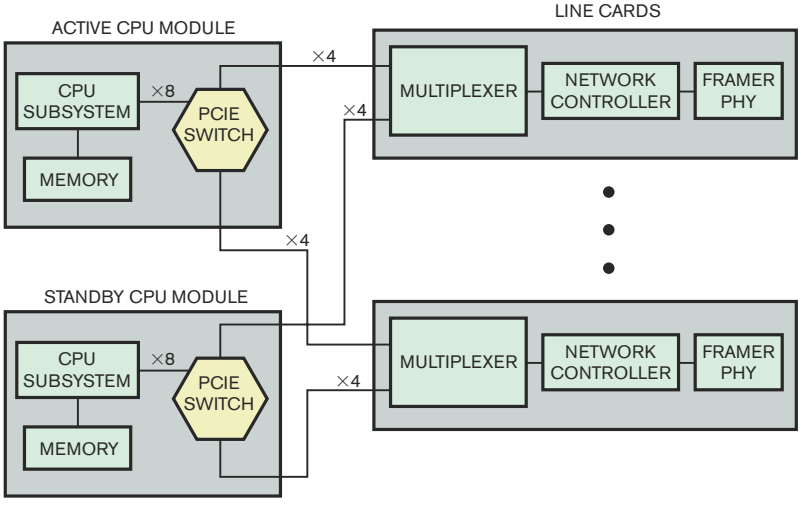


Figure 3 Implementing high reliability with the current version of PCI Express, which allows only one master processor, may require the use of multiplexers to isolate redundant processors (courtesy IDT).

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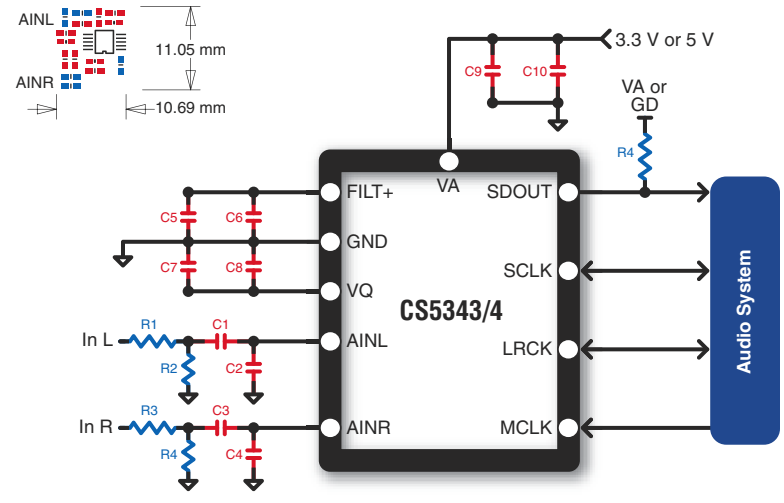
Actual Size:

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| Part | Resolution | Dynamic Range | THD+N | Sample Rate | Analog Inputs | Power Supply | Comments | Package |
|---|---|---|---|---|---|---|---|---|
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| CS5340 | 24 bits | 101 dB | –94 dB | 192 kHz | Single-ended | VA = 3.3 V or 5 V; VD = 3.3 V or 5 V; VL = 1.8 V to 5 V | Pin compatible with CS5341 | 16 TSSOP |
| CS5341 | 24 bits | 105 dB | –98 dB | 192 kHz | Single-ended | VA = 3.3 V or 5 V; VD = 3.3 V or 5 V; VL = 1.8 V to 5 V | Pin compatible with CS5340 | 16 TSSOP |
| CS5342 | 24 bits | 105 dB | –98 dB | 192 kHz | Single-ended | VA = 3.3 V or 5 V; VD = 3.3 V or 5 V; VL = 2.5 V to 5 V | 384*Fs MCLK | 16 TSSOP |
| CS5345 | 24 bits | 104 dB | –95 dB | 192 kHz | Single-ended | VA = 3.3 V or 5 V; VD = 3.3 V or 5 V; VLS = 1.8 V to 5 V; VLC = 1.8 V to 5 V | input mux, PGA, mic pre-amp | 48 LQFP |
| CS5351 | 24 bits | 108 dB | –98 dB | 192 kHz | Single-ended | VA = 5 V; VD = 3.3 V or 5 V; VL = 2.5 V to 5 V | Functionally compatible with CS5361 | 24 SOIC 24 TSSOP |
| CS5361 | 24 bits | 114 dB | –105 dB | 192 kHz | Differential | VA = 5 V; VD = 3.3 V or 5 V; VL = 2.5 V to 5 V | Pin compatible with CS5381 | 24 SOIC 24 TSSOP |
| NEW CS5364/66/68 | 24 bits | 114 dB | –105 dB | 192 kHz | Differential | VA = 5 V; VD = 3.3 V to 5 V; VLS/VLC = 1.8 V to 5 V | 4-/6-/8-Channel ADC, TDM, on-chip oscillator | 48 LQFP |
| CS5381 | 24 bits | 120 dB | –110 dB | 192 kHz | Differential | VA = 5 V; VD = 3.3 V or 5 V; VL = 2.5 V to 5 V | Flagship performance | 24 SOIC 24 TSSOP |




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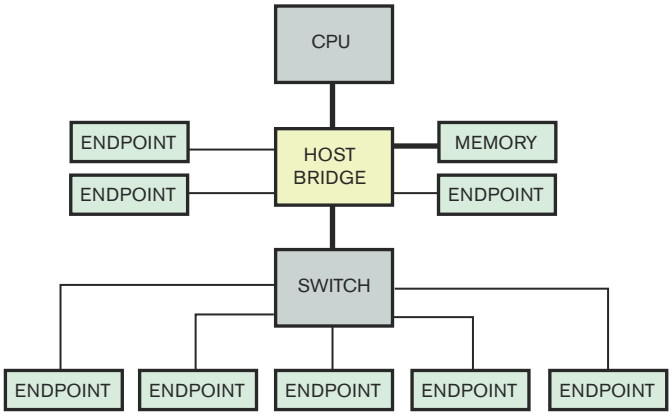
root processor initializes and enumerates the resources in its complex so that it can communicate with them through memory accesses. If two root processors were sharing the same bus, the two would generate conflicting address maps. By providing address translation, the switch effectively hides the existence of one root CPU from the other and allows each root CPU to use the address mapping that it generated to access the resources. The switch also resolves contention for resources. The major drawback of the nontransparent bridge is that no standard for its implementation exists. Thus, each vendor's product has its own unique software impact.

The limitations of PCIe in a data-plane application make it a weak contender for replacing proprietary fabrics in this aspect of communications designs. Yet, the economic factors that prompted interest in PCIe have begun to initiate a replacement of proprietary fabrics. The replacement is typically switched Ethernet.

Ethernet also represents a technology that enjoys lower cost based on high volume. Further, it offers a standardized way of implementing communications from multiple hosts to shared endpoints. It also has substantial data-handling capacity; 10-Gbps switch devices from Fulcrum Microsystems are on the market. A host of products provides bridges from Ethernet to other communications protocols, simplifying the design of a multiprotocol system. These attributes have begun prompting communications-system vendors to begin designing access-tier systems, such as DSLAMs (digital-subscriber-line-access multiplexers) using PCIe for the control plane and switched Ethernet for the data plane.

Supporters of PCIe point out, however, that the economics and performance road map of PCIe may eventually push Ethernet, as well as proprietary fabrics, off the data plane. The high volume of Ethernet production is currently in the 1-Gbps devices. PCIe now offers eight- and 16-lane devices, offering data rates as high as 40 Gbps, which vendors developed for the graphics needs of PCs. PCIe supporters see that technology quickly becoming available for switches, bridges, and additional endpoint peripherals.




PCI Express replaces the parallel PCI bus with switched serial links containing one or more lanes (courtesy Intel).

Still, these products represent only a potential. Currently, only a few PCIe devices on the market do not specifically target PC and graphics applications. These products include mostly switches and bridges. Companies such as IDT, NEC, Texas Instruments, and PLX Technology are offering both transparent and nontransparent switches ranging from two-port, four-lane devices to eight-port, 48-lane devices. PCIe bridges are also available from these companies, as well as from AMCC, Intel, and others. The bridges include both upstream and downstream connections between PCIe and PCI, PCI-X, and Ethernet.

Opportunity also exists on the custom-design front. FPGA devices from Lattice Semiconductor are available with PCIe interface cores from Northwest Logic and PHY (physical)-layer components from Genesys Logic. NEC also offers PCIe cores, including controller and PHY cores. Even the EDA vendors have started getting into the custom-PCIe market, with Cadence offering both design IP (intellectual proprerty) and verification tools for PCIe designs.

**MORE AT EDN.COM**

**For more on PCI Express, visit www.edn.com/article/CA601851.**

**For Contributing Technical Editor Richard Quinnell's recent article "Clash of the wireless-USB standards," go to www.edn.com/article/CA6363903.**

With the current emphasis in the market on PCs and graphics applications, the use of PCIe in communications designs is still at its earliest stages. The potential is there, however, in both architecture and performance, to fill many niches in communications control. The efforts of the PCI-SIG and individual companies to address the architectural mismatches that still exist between the processor-centric PC and data-centric needs of communications systems will only improve the situation. PCIe may not dominate communications-system designs, but it could well become a strong player in that market. EDN

## AUTHOR'S BIOGRAPHY

*Contributing Technical Editor Richard A Quinnell has been covering technology for more than 15 years after an equally long career as an embedded-system-design engineer.*

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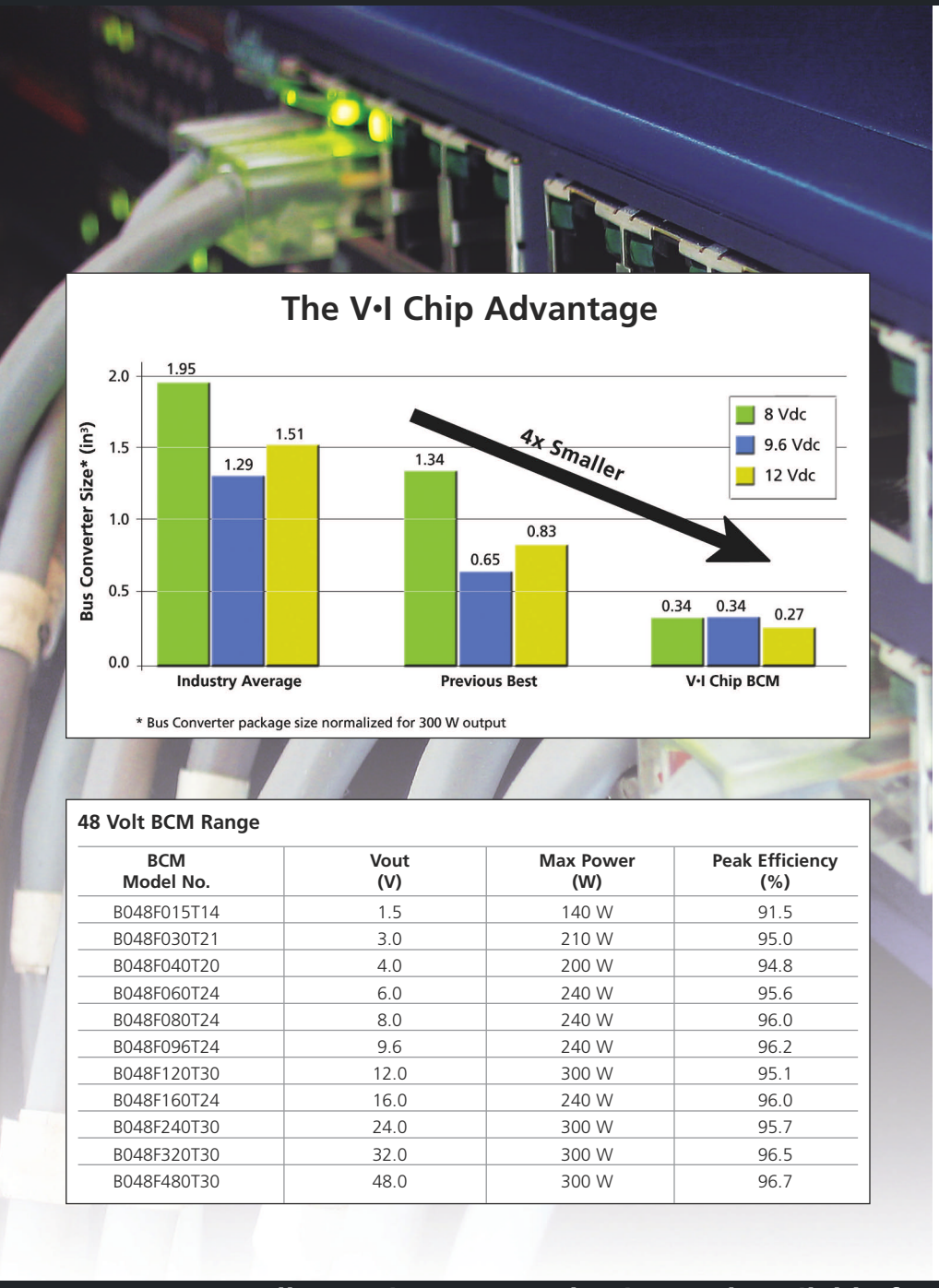

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* Bus Converter package size normalized for 300 W output

**48 Volt BCM Range**

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|---|---|---|---|
| B048F015T14 | 1.5 | 140 W | 91.5 |
| B048F030T21 | 3.0 | 210 W | 95.0 |
| B048F040T20 | 4.0 | 200 W | 94.8 |
| B048F060T24 | 6.0 | 240 W | 95.6 |
| B048F080T24 | 8.0 | 240 W | 96.0 |
| B048F096T24 | 9.6 | 240 W | 96.2 |
| B048F120T30 | 12.0 | 300 W | 95.1 |
| B048F160T24 | 16.0 | 240 W | 96.0 |
| B048F240T30 | 24.0 | 300 W | 95.7 |
| B048F320T30 | 32.0 | 300 W | 96.5 |
| B048F480T30 | 48.0 | 300 W | 96.7 |


32.5 x 22.0 x 6.6 mm
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BY MICHAEL SANTARINI • SENIOR EDITOR

WITH RESOURCES AND NEW BUSINESS STRETCHED ACROSS THE GLOBE, DESIGN MANAGERS ARE EMPLOYING A RANGE OF METHODS TO GET DESIGNS DONE ON TIME.

# ASIC-design managers face GLOBAL CHALLENGES

With the emergence of IC foundries in Taiwan, Singapore, and mainland China over the last decade and an abundance of relatively inexpensive engineering resources in India, Eastern Europe, and mainland China now available, ASIC and SOC (system-on-chip) design is becoming a global effort. Indeed, it is difficult to find a company that has not established an offshore design center or is not tapping into a foreign location for some type of assistance, whether it is for manufacturing a chip at a Taiwanese fab, design services in India, or IP (intellectual-property) creation in Israel.

An abundance of global resources is available to IC companies. But that abundance brings numerous challenges that management must face in organizing ASIC- and SOC-design efforts to get chips to market on time. Global efforts require managers to negotiate different time zones, language, cultures, holiday schedules, licensing, and infrastructure. Beyond these issues, design managers are coming up with unique strategies to ensure that designs meet goals and are on time. To complete designs on time, they use localized R&D with global manufacturing, global-platform-based design, and global-design factories.

## LOCALIZED R&D

Raza Microelectronics is perhaps the epitome of the localized R&D company. A Silicon Valley start-up that has raised approximately $120 million in venture-capital funding, Raza Micro is producing complex 300 million-transistor SOCs for the 3G base-station and security-appliance markets. The company has resisted the temptation to tap into relatively less expensive offshore hardware-engineering resources. It has even resisted the appeal of nationally distributed design teams. "At Raza Micro's XLR-processor line, we don't develop typical ASICs, so the model for a typical ASIC doesn't work for us," says Nazar Zaidi, vice president of engineering for scalable processors at Raza. "We need to have tight integration of the various aspects of the design. That means we must have close geometric proximity of the different types of IC designers."

All of Zaidi's hardware-design team is in Cupertino, CA. "Having design teams split further exacerbates the time-to-market problem," Zaidi says. "If we were dealing with standard, proven methodologies, processes, and everything else, then we could think about separating and farming out work here and there, but, more often than not, we're trying to solve a difficult technical challenge as we are building the chip. We don't have all the answers when we start out. We expect to find the answers as we are working on it, so there is not a lot of time to create a detailed methodology and flows that we can hand off to an offsite team." A significant percentage of Raza Micro's designs require full-custom

techniques, though the company mixes in more automated-ASIC methods and IP when it can. "What we think may be custom on day one may change based on how the design evolves," Zaidi says. In the course of a given chip-design project, the size of a team varies from 20 to 65 engineers, and the team grows to its largest during layout.

The company has small groups that specialize in one aspect of the design-logic design, verification, or layout and DFM (design for manufacturing), but employees with broad repertoires are key. "In a start-up, you have to have individuals that can wear many hats; those folks tend to be the glue of the team," Zaidi says. "They are the ones that make sure that information transfers accurately from one group to the other because they understand the issues on both sides." Although Raza's hardware team is in one location, the company has a software-development group in India. "Software design starts typically a couple of months after hardware design begins," Zaidi says. "There are some severe limitations. We run a lot of applications on RTL [register-transfer level] long before we tape out the chip. We have performance and reference models in which we run large blocks of field software code to see how parts of the machine will behave and react."

## AT A GLANCE

- Raza Microelectronics has all of its hardware engineers in one location.
- Pixelworks leverages creativity in its groups worldwide using a platform approach.
- Open Silicon tightly constrains every aspect of design, seemingly allowing it to establish groups anywhere in the world.
- Traditional ASIC vendor Infineon's ADS (ASIC Design and Security) Group has global design teams serving local customers.
- Traditional ASIC vendor NEC America concentrates on clients in North America but finds customers are using global resources to do front-end design.

The company uses TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) to manufacture its silicon and gets the foundry involved early in the process. "Our chip was one of the first high-performing processors TSMC fabbed in its 90-nm process," says Zaidi, noting that Raza is currently targeting its next-generation ICs at TSMC, as well, but Zaidi declines to disclose at which node. Raza Micro also buys IP from various sources. The company holds a MIPS (www.mips.com)-processor-architecture license but does not buy predefined cores from MIPS. The company also acquires commodity IP for standard functions. "Designing a new UART is not necessarily the value we provide in the chip, so we acquire some standard IP from vendors," says Zaidi.

As Raza Micro grows, the company puts more effort into global design, depending on the complexity of the design. "There are capable resources in China, India, and Eastern Europe," says Zaidi. "When you get into the second or third level of derivatives, then maybe you can give a full design to those folks. If you outsource, you should outsource the whole thing. You don't want to draw boundaries between glue logic, circuits, physical design, and all that; you have to hand it off as a full-blown project."

## PLATFORM APPROACH

Whereas Raza Micro uses a localized R&D design effort with globalized software design and manufacturing, publicly held system company Pixelworks has embraced global design by employing a platform-based approach. Chief Technical Officer and Vice President of Engineering Richard Tobias manages a few hundred engineers in several design centers in North America, Asia, Western Europe, and Eastern Europe. The company has four product lines, with

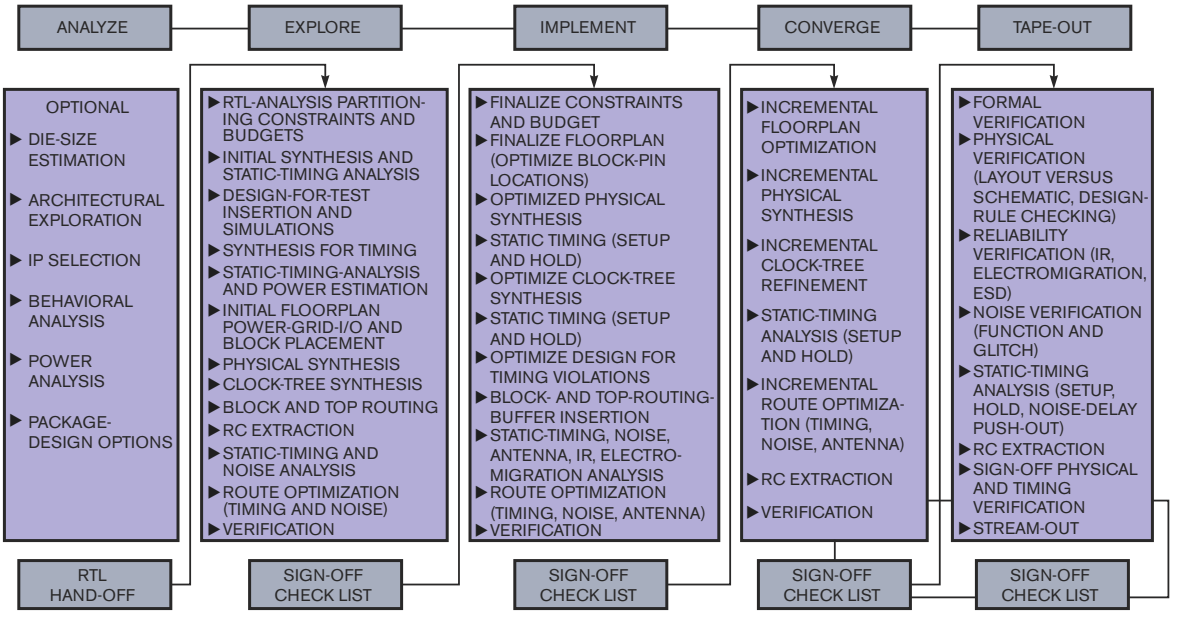


Figure 1 Open Silicon uses a fixed methodology for all its designs.

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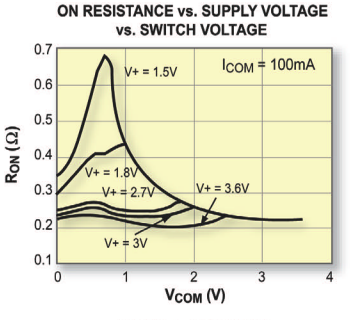
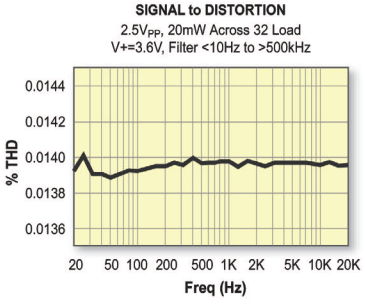
| | Device | Function | $R_{ON}$ @ 2.7V (Ω) | $R_{ON}$ Flatness (Ω) | ESD (HBM) | Supply Voltages (V) | Packages |
|---|---|---|---|---|---|---|---|
| Singles | ISL84714 | SPDT/2:1 Mux | 0.44 | 0.06 | 6kV | 1.6 to 3.6 | SC70-6 |
| | ISL84715 | SPST (NO) | 0.26 | 0.04 | 4kV | 1.6 to 3.6 | SC70-5 |
| | ISL84716 | SPST (NC) | 0.26 | 0.04 | 4kV | 1.6 to 3.6 | SC70-5 |
| | ISL43L210 | SPDT/2:1 Mux | 0.44 | 0.06 | 6kV | 1.1 to 4.5 | SC70-6 |
| | ISL43L110 | SPST (NO) | 0.26 | 0.04 | 4kV | 1.1 to 4.5 | SC70-5 |
| | ISL43L111 | SPST (NC) | 0.26 | 0.04 | 4kV | 1.1 to 4.5 | SC70-5 |
| Duals | ISL84762 | 2xSPDT/2:1 Mux | 0.29 | 0.03 | 9kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL84684 | 2xSPDT/2:1 Mux | 0.29 | 0.03 | 9kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL8484 | 2xSPDT/2:1 Mux | 0.29 | 0.03 | 9kV | 1.6 to 4.5 | TDFN, MSOP |
| | ISL43L220 | 2xSPDT/2:1 Mux | 0.23 | 0.03 | 9kV | 1.1 to 4.5 | TDFN |
| | ISL43L410 | DPDT/Diff 2:1 Mux | 0.29 | 0.03 | 9kV | 1.1 to 4.5 | TDFN, MSOP |
| | ISL43L120 | SPST (NO) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L121 | SPST (NC) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L122 | SPST (Mix) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L710 | Diff SPST (NO) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L711 | Diff SPST (NC) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| | ISL43L712 | Diff SPST (Mix) | 0.17 | 0.008 | 8kV | 1.6 to 3.6 | TDFN, MSOP |
| Quads | ISL83699 | Dual DPDT/Diff 2:1 Mux | 0.3 | 0.06 | 9/4kV | 1.6 to 3.6 | QFN, TSSOP |
| | ISL84780 | Dual DPDT/Diff 2:1 Mux | 0.45 | 0.07 | 4kV | 1.6 to 3.6 | TQFN, TSSOP |
| | ISL8499 | Dual DPDT/Diff 2:1 Mux | 0.3 | 0.06 | 9/4kV | 1.6 to 4.5 | QFN, TSSOP |
| | ISL43L420 | Dual DPDT/Diff 2:1 Mux | 0.3 | 0.06 | 9/4kV | 1.1 to 4.5 | QFN |
| Octals | ISL84781 | 8:1 Mux | 0.41 | 0.056 | 4kV | 1.6 to 3.6 | TQFN, TSSOP |
| | ISL84782 | Diff 4:1 Mux | 0.5 | 0.056 | 4kV | 1.6 to 3.6 | TQFN, TSSOP |
| | ISL43L840 | Dual 4:1 Mux | 0.5 | 0.056 | 4kV | 1.6 to 3.6 | QFN, TSSOP |
| | ISL43L841 | Diff: 4:1 Mux | 0.5 | 0.056 | 4kV | 1.6 to 4.5 | TQFN, TSSOP |

## ISL84684 Typical Performance

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engineering groups for each line producing two to four chips per year. "Most chips are derivatives," says Tobias. "Few chips are developed in just one location. IP from groups around the world come together in one design center to create a system chip."

Pixelworks has adapted a concise platform-based approach for its IC designs to make sure it just isn't slapping disparate blocks together in the 11th hour of the design process. It's an approach Tobias helped devise at his previous company, Toshiba (www.toshiba.com), which developed the SOCMosaic platform, and is an approach that TI (www.ti.com) has successfully employed with its OMAP (Open Multimedia Applications Platform) product. "In the platform approach, the platform architecture is the same for every SOC, but some of its chips are not really SOCs," says Tobias. "Every chip family is its own market-segment-oriented product line. You can use the generic platform to generate any SOC, but you need market-specific IP, software, systems knowledge, and so forth to create a specific chip."

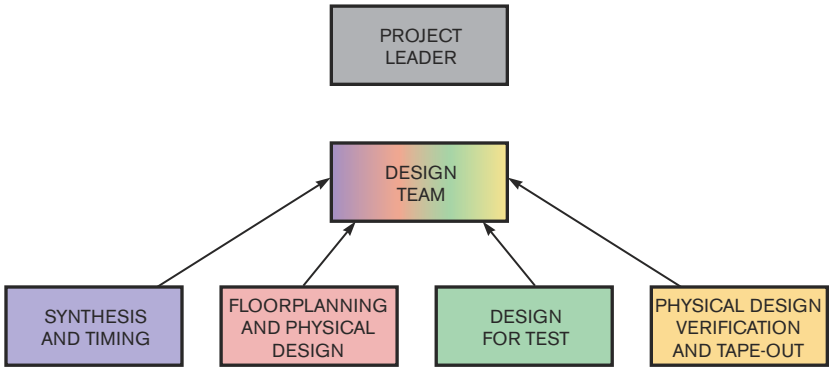


Figure 2 Open Silicon organizes design groups into design-control units, in which each member specializes in one area of design. Open Silicon rotates members of these units to ensure that "fiefdoms" don't develop within the organization.

An SOC-block-based development architecture, such as a platform, allows global teams to simultaneously develop designs and to work on the same chip. "For complicated chips, you need to find expertise for subfunctions in many parts of the world," Tobias says. "You then need to combine the IP they create into a bigger system—boards, chips, and software. You need to create an architecture that makes it easy to do this co-development without a huge amount of interaction between the groups. So, we've created a system architecture that predefines the interfaces, thus allowing the teams to interact only across this API [application-programming interface] or chip interface, and thus we can quickly create systems."

The company's architecture group develops each product line and platform. "This group creates the overall architecture and creates the methodologies and tool flows to design in the architecture," says Tobias. "This sort of architecture is generic for SOCs. Each product line then has a system architecture. A local architect with the local chip team leads this architecture development, but the global architecture group does most of the software development because most of the company's software is portable to every platform."

Although the company has design teams focus on particular projects, the verification team is a separate organization but has people in every design center. "Most system verification is in a single site, but unit verification typi-

## GUIDE TO GLOBAL DESIGN

**Open Silicon's co-founder, president, and chief executive officer, Naveed Sherwani, PhD, offers six guidelines for global design that his company follows:**

**• You need a sophisticated and well-trained project-management staff–a tricky goal to accomplish. It involves issue control, schedule handling, and cost handling. Hence, it is difficult to hire staff for and to manage.**

**• Let talent, rather than cost, drive your push toward globalization. Looking for talent in Taiwan, Israel, or India can help you with your projects. Cost can increase if you lack the necessary talent.**

**• Automate your processes by developing process-management software, such as Open Silicon's IC Catalyst. The program helps the company standardize the design from the start of the process to delivery of a prototype. It handles all the processes, schedules, cost, people, and tool issues.**

**• Standardize processes. If you come up with a new process for every project, you will fail. The projects you do successfully on a global scale are truly standardized. Use a version of Open Silicon's DCUs (design-control units)–highly standardized ASIC processes. In such a unit, all participants know what to do and can apply the same process to multiple projects and then use a system to automate and relay it to others.**

**• Create a culture within the company of working around the clock. This rule must come from top management. You, all your executives, and their subordinates must be willing to attend meetings in the middle of the night. It's hard, and a lot of companies struggle with it. If they can't attend meetings at 8 a.m. or after 5 p.m. or are unwilling to occasionally work on weekends, they can't be part of a global team. Otherwise, the people in Israel, India, or Taiwan need to have meetings in the middle of the night. All team members must have the same work ethic.**

**• Understand the cultural issues of different countries. Israel works in different ways from India and the United States, and European teams work differently from US teams. Some cultural barriers, challenges, and advantages crop up. In India, for example, it is common for people to come to work at 9 or 10 a.m. versus 7 or 8 a.m., but it's also common to work late into the night.**

# Intersil Voltage References

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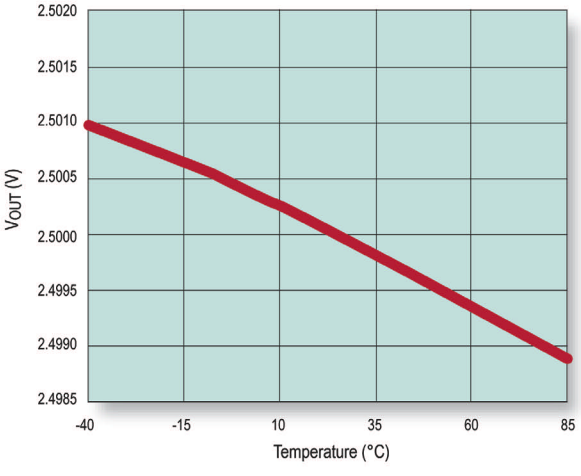
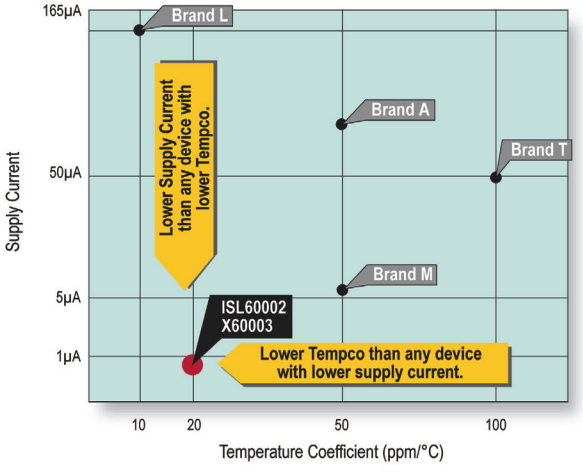
**VOUT ACCURACY vs TEMPERATURE NORMALIZED TO 25°C (Output = 2.5V)**




**TEMPERATURE COEFFICIENT vs SUPPLY CURRENT**




**ISL60002 and X60003 Key Parameters**

| Description | Conditions | Device Grade | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| Initial Accuracy | @25°C | B | -1.0 | | +1.0 | mV |
| | | C | -2.5 | | +2.5 | mV |
| | | D | -5.0 | | +5.0 | mV |
| Tempco | -40°C to +85°C | | | | 20 | ppm/°C |
| Supply Current | -40°C to +85°C | | | 350 | 700 | nA |
| Input Range | -40°C to +85°C | | 2.7 | | 5.5 | V |
| Long Term Drift | ΔTA = 25°C | | | 10 | | ppm/√1kHrs |

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cally happens closer to the developer," says Tobias. "We try to keep unit tests near the unit developer and system tests near the system developer."

The company collocates most firmware development with the hardware teams, but system-software development typically occurs at other sites. "We develop higher level application software as subfunctions in a way that allows worldwide development," says Tobias. The biggest key to employing the global-platform-based approach is having great site management, he says. "You need to pick global leaders. Your leadership can be in many countries, but they need to be special people who took the time to understand many worldwide cultures. We also have global program managers with the same sort of leadership skills," Tobias says.

To keep track of designs, Pixelworks has a program office and has created a standard set of methodologies and flows to manage projects. A set of standard reports sums up these projects so that upper management can track all programs—both global and local—in the organization. The company has also established a standard EDA flow across its organization based on best-in-class point tools from EDA vendors. Tobias notes that EDA companies could further help his organization by creating better program-management tools and EDA-database-management tools that work worldwide.

Pixelworks develops most of its own IP but sometimes procures it from IP vendors. However, the company tries to steer clear of IP licensing that demands royalties. "We have great ideas from our multinational teams. We need teams that are big enough to allow for interaction and with enough engineering disciplines that the group can create ideas. Also, communication is key. Creating a highly communicative environment involves using tools from conference calls, videoconferences, screen sharing, and database sharing."

Whereas Raza Microelectronics prefers to have all its hardware engineers in one location and Pixelworks uses engineering talent around the globe in the framework of a platform approach, Open Silicon has introduced a highly

## ASIC HOUSES CHANGE WITH THE GLOBAL TIDE

**Design groups in systems companies are becoming more global, and so are many of the large traditional ASIC houses. ASIC houses such as Infineon and NEC have always worked with clients in other countries, receiving RTL (register-transfer-level) hand-offs from international sources; now, they are increasing their use of global work forces but employing new strategies.**

**For example, Infineon's ADS (ASIC Design and Security) business unit has 130 engineers, largely in Europe and Asia. Armin Stolze, worldwide director of the ADS unit, manages the team, which has 30 employees in Singapore, 50 in Germany, 30 in Austria, and 20 in China. The Chinese group is still in its ramp-up phase. Each location specializes in different aspects of design. The Austrian group focuses on analog- and mixed-signal-design development and works with customers worldwide. The other three locations focus regionally on SOC (system-on-chip) design. "Our strategy is to have our design teams work closely with our customers," says Stolze, noting that the Chinese and Singaporean teams work with customers in Asia, and the German group typically works with customers in Europe and North America.**

**When possible, Stolze prefers to have teams complete designs in one location that is geographically closest to the customer. However, this scenario is sometimes impossible because of lack of resources or lack of expertise at a certain location, he says.**

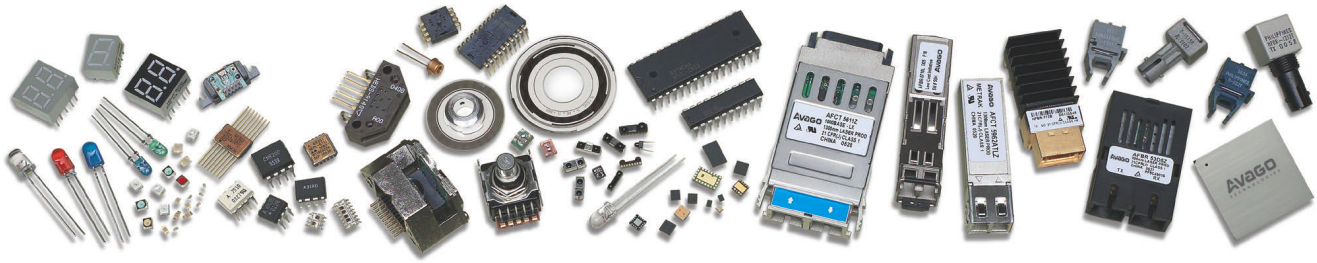
**The Austrian team usually develops analog- and mixed-signal functions as macros with all the necessary views to allow its SOC center to integrate the macros into the SOC. "For SOC design, it is challenging to divide the task, so there is a minimum of daily hand-off between the teams," says Stolze. "A large SOC requires the participation of multiple sites or experts. One site typically takes ownership of the top-level design and then divides up the blocks to specialty groups or experts to minimize the daily hand-over between groups."**

**NEC is also a global company, but its North American ASIC group has design centers in Santa Clara, CA; Portland, OR; Boston; and Chicago. John Fallin, executive director of engineering for NEC Electronics America's custom-SOC business unit, says that each of his groups serves regional customers. "We don't by design try to localize abilities in certain locales," he says, noting that this situation sometimes occurs, however. "We try to find the most capable people available for the time frame of that project. Sometimes, we do a bit of shuffling to get the right people on a project." He claims that you can get away with less documentation and less project management if you have everyone sitting in the same room. However, he adds, "With complex designs, you can run into a lot of messes even if everybody is sitting in the same cube. We are geographically dispersed for a lot of good reasons–one being that we have customers who are geographically dispersed, and so it's good to have engineers locally with customers."**

**Increasingly, NEC America's customers have their own logic-design groups or are using foreign design services to develop the RTL, which means Fallin's group is becoming more global, whether or not it wants to. "We have been working for a long time with our colleagues in Japan and working over that nine- to 12-time-zone difference," says Fallin. "Over the last five to 10 years, we've worked to build a robust product-management methodology, mindset, and culture. By using these factors, these geographical differences become less of an issue."**

# Your system

# Our solutions



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- Consumer Appliances
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## GLOBAL DESIGN FACTORY

Unlike Raza and Pixelworks, Open Silicon is not a systems company. Instead, it is a fabless-ASIC vendor, a new breed that works with foundries to produce silicon using RTL or netlist hand-offs (see **sidebar** "ASIC houses change with the global tide"). It then performs package design and testing. There are a handful of fabless-ASIC vendors in the market today, but Open Silicon differentiates itself by employing a highly disciplined design model that it believes exceeds global boundaries. The company's co-founder, president, and chief executive officer, Naveed Sherwani, PhD, was formerly the general manager of Intel's (www.intel.com) now-defunct ASIC business; through that experience and others, he derived Open Silicon's unique model. "In the three years at Intel, we had 28 design wins, and in the three years since we've founded Open Silicon, we have 70 design wins," says Sherwani. "I believe that is the most that any ASIC vendor produced in recent years." The company's revenue will grow this year to nearly triple that of last year. The company owes its success in a small part to hiring relatively inexpensive labor in India and largely to enforcing great discipline and parameters on the types of ASICs the company will design and even more discipline in how it designs them. The company manufactures only relatively simple, mainstream ASICs. It does not bother with complex analog- or mixed-signal designs or super-high-performance digital designs in the most advanced process geometries. The company engages only those projects that meet its "22-point criteria." For example, one criterion is that the design team can implement the design in 180- to 90-nm process geometries; another is that the design must have no more than 20 million gates. The company has similar criteria for hierarchy, amount of memory, and number of IP blocks in a design. The company has developed and enforces a strict internal methodology, using one tool flow across all design groups (**Figure 1**).

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For more on team design, see Executive Editor Ron Wilson's recent article at www.edn.com/article/CA6347251.

Go to www.edn.com/061012df1 and click on Feedback Loop to post a comment on this article.

The company divided its engineering force into DCUs (design-center units). "It is a simple concept that simply states: 'Constrain yourself to doing certain types of ASICs,'" says Sherwani. "We've created a systematic, methodical flow in which the steps don't change; hence, over time, you can automate as much as possible. It allows us to create multiple such DCUs around the world, so we don't have to worry that designers in Israel are doing a design differently from those in India. You have a cookie-cutter DCU that you can put anywhere in the world."

A DCU at Open Silicon comprises five or six engineers (**Figure 2**). Each engineer specializes in a discipline of layout or physical verification. Sherwani notes that, in large ASIC groups, "fiefdoms" often develop within engineering staffs, and designers form into an A Team, a B Team, and a C Team. To avoid this scenario, Sherwani rotates engineers within DCUs. The company has a profile of the types of engineers it will hire, typically tapping into second- and third-tier universities in India to find overlooked talent. The company has also developed its own IC Catalyst management software, which allows it to standardize the design from the start of the process to delivery of a prototype. IC Catalyst handles all the processes, schedules, cost, people, and tool issues. The tool controls versions of EDA software, too. The company has derived a point-tool flow from the various EDA-vendor flows and has strict rules on their use.

Although Open Silicon can implement DCUs anywhere in the world, the company resists increasing its staff and wants to make its engineering staff more productive by increasing the amount of automation in its organization and tool flow. "We're focused on optimizing existing designs rather than initiating new, labor-intensive designs," says Sherwani. "You'll not see our head count go from 100 people to 5000 people. The idea is to use the optimized methods to do more designs with the same number of people. We will grow, and we plan on investing more in our current infrastructure so that we become more productive. That rapid growth model—one design with 100 people and the next design with 400 people and the next with 800 people—is a formula for death. When I was at Intel, we were using 1200 people for a single ASIC, and 400 people were doing nothing but coordinating other people." Sherwani offers six rules the company follows for global design (see **sidebar** "Guide to global design").

Overall, chip-design companies are employing many innovative strategies to leverage global resources. Although some debate exists about whether companies can effectively create highly complex ASICs and SOCs—R&D-class designs that break new ground in performance or features—on a global scale, everyone concurs that worldwide engineering resources and talent are growing, and new market opportunities are on the horizon. It will be interesting to watch what new methodologies develop as China and India mature and make the inevitable transition from centers of low-cost manufacturing to powerhouses in IC-design innovation. If you don't believe that this transition will take place, visit Shanghai; it will take you less than a day to realize that it already has. EDN

## FOR MORE INFORMATION

**Infineon Technologies**
**ASIC Design and Security Group**
www.infineon.com

**NEC Electronics America**
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**Pixelworks**
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**Raza Microelectronics**
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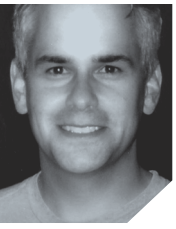
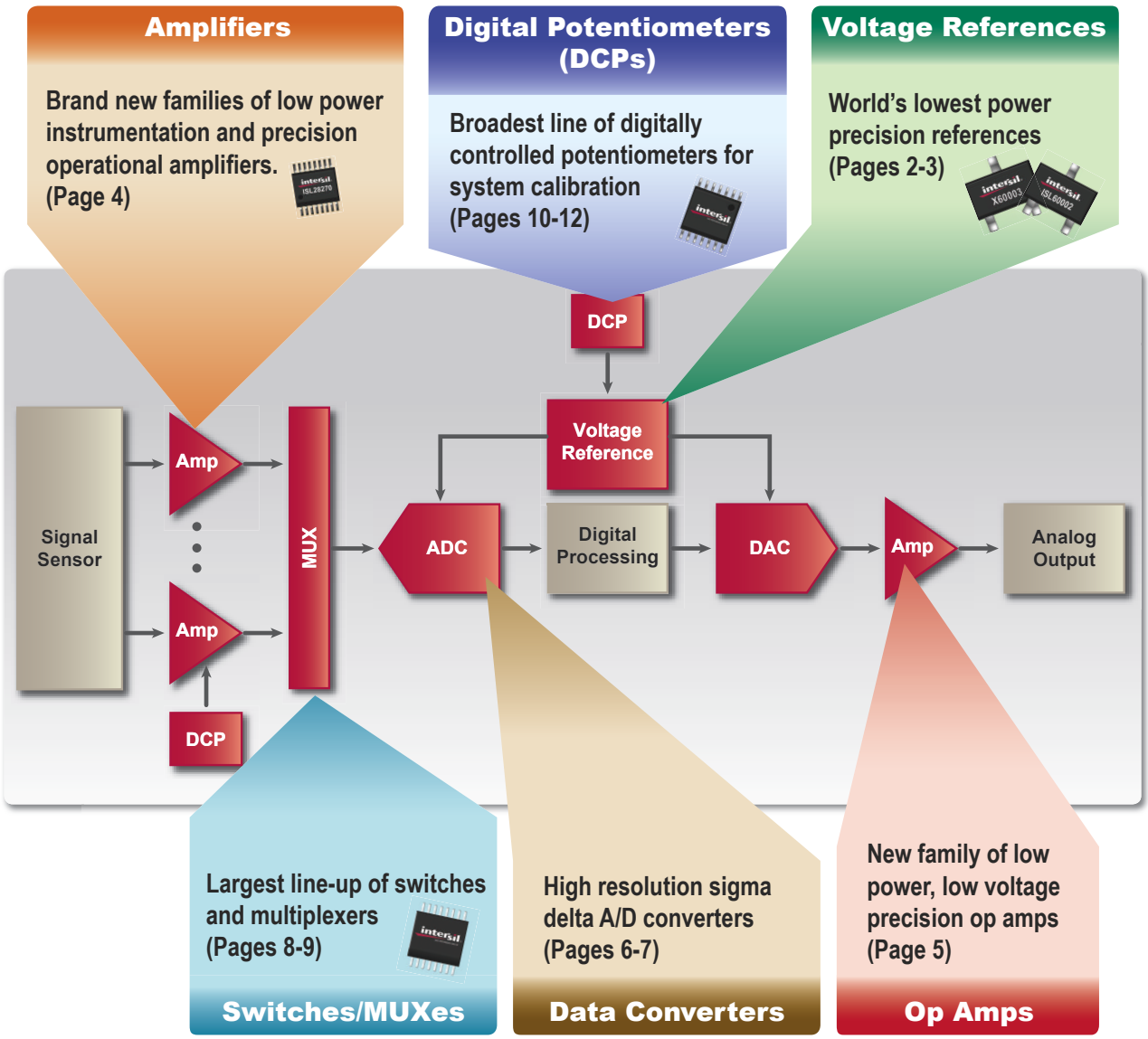


# When Stability and Accuracy are Important You Can Count on Intersil's Precision Analog ICs



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Intersil's ISL60002 and X60003 deliver initial accuracy as low as ±1mV on just 700nA max supply current. Choose from a wide range of output voltages including: 1.024, 1.2, 1.25, 1.8, 2.048, 2.5, 3.3, 4.096, and 5.0V.

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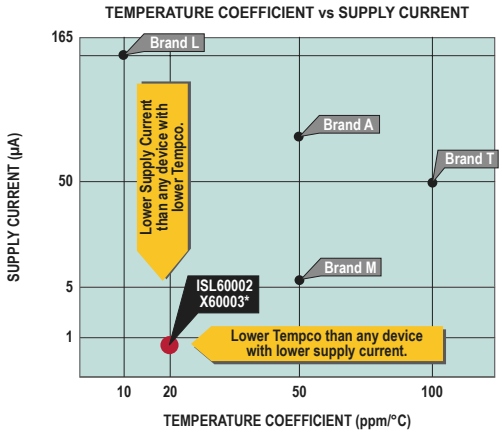
Excellent stability over industrial temperature range.




* Tempco on B grade of X60003 is 10ppm/°C

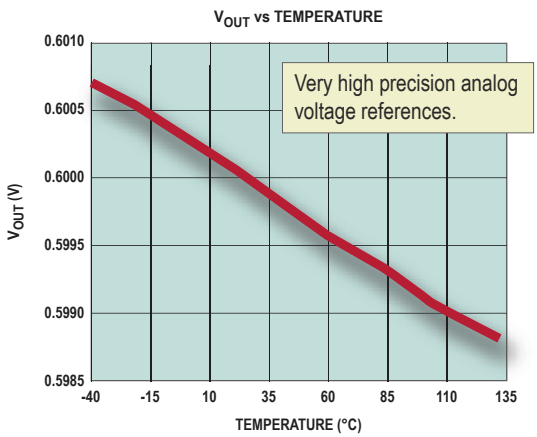
## ISL60002 and X60003 Key Parameters

| Description | Conditions | Device Grade | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Initial Accuracy | @ 25°C | B | -1.0 | | +1.0 | mV |
| | | C | -2.5 | | +2.5 | mV |
| | | D | -5.0 | | +5.0 | mV |
| Tempco | -40°C to +85°C | B, C, D | | | +20* | ppm/°C |
| Supply Current | -40°C to +85°C | B, C, D | | +350 | +700 | nA |
| Input Range | -40°C to +85°C | B, C, D | +2.7 | | +5.5 | V |
| Long Term Drift | $\Delta T_A$ = +25°C | B, C, D | | +10 | | ppm/√1kHrs |

* Tempco on B grade of X60003 is 10ppm/°C

# Industry's Best Temperature and Time Drift Performance Among Sub 1.0V Voltage References

Intersil's ISL21032 offers 0.6V output without sacrificing accuracy over temperature and time.





## Key Features

- 0.6V output voltage
- World-beating absolute accuracy from -40°C to +130°C
  - Three grades available: ±0.5%, ±0.75%, ±1%
- Ultra-low supply current: 25µA
- Excellent long-term stability: 10ppm/√kHrs
- Tiny SOT-23 package

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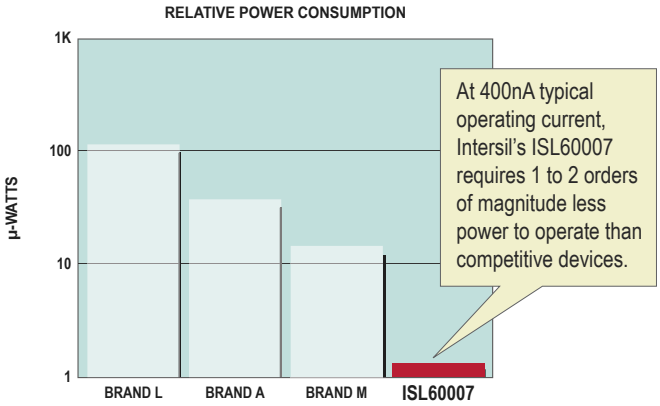
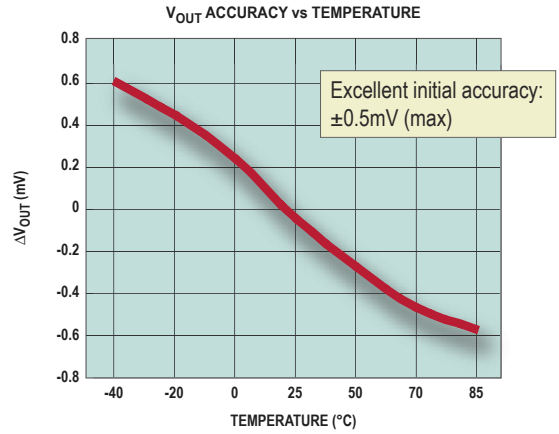
Intersil's ISL60007 delivers the industry's best accuracy on just 800nA typical operating current.


- $V_{OUT}$ .....2.5V
- Very low supply current.....800nA (max)
- Long-term drift ..... 10ppm/√1kHrs
- Superior tempco .....3ppm/°C
- Output drive capability ..... ±7mA
- Input range..... 2.7V to 5.5V

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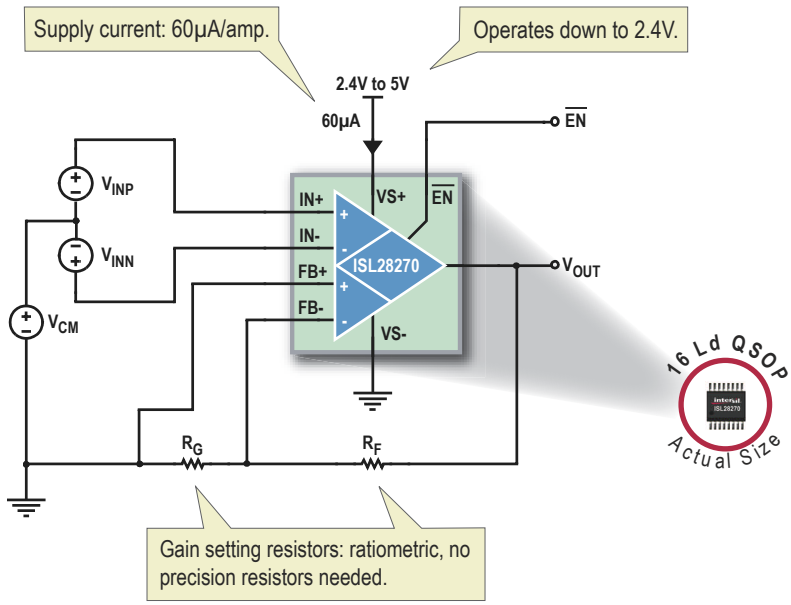
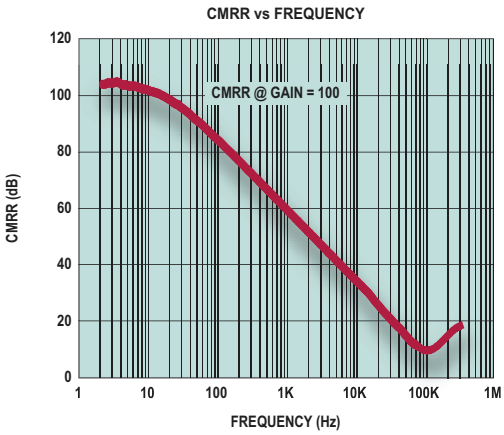
| Part Number | Input (V) | $V_{OUT}$ (V) | Initial Acc. (mV) | Tempco (ppm/°C) | $I_{SS}$ | LTD (typ) (ppm) | Hyst. (ppm) | $e_N$ (typ) ($\mu V_{PP}$) | Temp. Range (°C) | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| ISL60002 | 2.7 to 5.5 | 1.024 | 1.0, 2.5, 5.0 | 20 | 700nA | 10 | 100 | 30 | -40 to +85 | 3 Ld SOT-23 |
| ISL60002 | 2.7 to 5.5 | 1.2 | 1.0, 2.5, 5.0 | 20 | 700nA | 10 | 100 | 30 | -40 to +85 | 3 Ld SOT-23 |
| ISL60002 | 2.7 to 5.5 | 1.25 | 1.0, 2.5, 5.0 | 20 | 700nA | 10 | 100 | 30 | -40 to +85 | 3 Ld SOT-23 |
| ISL21009* | 3.5 to 16.5 | 1.25 | 0.5, 1.0, 2.0 | 3, 5, 10 | 160µA | 10 | 50 | 4 | -40 to +125 | 8 Ld SOIC |
| ISL60002 | 2.7 to 5.5 | 1.8 | 1.0, 2.5, 5.0 | 20 | 700nA | 10 | 100 | 30 | -40 to +85 | 3 Ld SOT-23 |
| ISL60002 | 2.7 to 5.5 | 2.048 | 1.0, 2.5, 5.0 | 20 | 700nA | 10 | 100 | 30 | -40 to +85 | 3 Ld SOT-23 |
| ISL60002 | 2.7 to 5.5 | 2.5 | 1.0, 2.5, 5.0 | 20 | 700nA | 10 | 100 | 30 | -40 to +85 | 3 Ld SOT-23 |
| ISL60007* | 2.7 to 5.5 | 2.5 | 0.5, 1.0 | 3, 5, 10 | 800nA | 10 | 50 | 30 | -40 to +85 | 8 Ld SOIC |
| ISL21009* | 3.5 to 16.5 | 2.5 | 0.5, 1.0, 2.0 | 3, 5, 10 | 160µA | 10 | 50 | 4 | -40 to +125 | 8 Ld SOIC |
| ISL21007* | 2.7 to 5.5 | 2.5 | 0.5, 1.0, 2.0 | 3, 5, 10 | 160µA | 10 | 50 | 4 | -40 to +125 | 8 Ld SOIC |
| X60008 | 4.5 to 6.5 | 2.5 | 0.5, 1.0 | 3, 5, 10 | 800nA | 10 | 50 | 30 | -40 to +85 | 8 Ld SOIC |
| ISL60002 | 3.5 to 5.5 | 3.3 | 1.0, 2.5, 5.0 | 20 | 700nA | 10 | 100 | 30 | -40 to +105 | 3 Ld SOT-23 |
| X60003 | 4.5 to 9.0 | 4.096 | 1.0, 2.5, 5.0 | 10, 20 | 900nA | 10 | 150 | 30 | -40 to +85 | 3 Ld SOT-23 |
| X60008 | 4.5 to 9.0 | 4.096 | 0.5, 1.0 | 3, 5, 10 | 800nA | 10 | 50 | 30 | -40 to +85 | 8 Ld SOIC |
| ISL21009* | 4.5 to 16.5 | 4.096 | 0.5, 1.0, 2.0 | 3, 5, 10 | 160µA | 10 | 50 | 4 | -40 to +125 | 8 Ld SOIC |
| X60003 | 5.1 to 9.0 | 5 | 1.0, 2.5, 5.0 | 10, 20 | 900nA | 10 | 150 | 30 | -40 to +85 | 3 Ld SOT-23 |
| X60008A | 5.1 to 9.0 | 5 | 0.5 | 1 | 800nA | 10 | 50 | 30 | -40 to +85 | 8 Ld SOIC |
| X60008 | 5.1 to 9.0 | 5 | 0.5, 1.0 | 5, 10 | 800nA | 10 | 50 | 30 | -40 to +85 | 8 Ld SOIC |
| ISL21009* | 5.5 to 16.5 | 5 | 0.5, 1.0, 2.0 | 3, 5, 10 | 160µA | 10 | 50 | 4 | -40 to +125 | 8 Ld SOIC |

* Coming Soon

# Rail-to-Rail Micropower Dual Instrumentation Amp Delivers Best Voltage Offset, Offset Voltage Drift, and Noise Performance

Intersil's new ISL28270 delivers 150µV max offset voltage on just 60µA $I_{SS}$ per Amp.




## Key Features

- Single supply operation: 2.4V to 5V
- Supply current: 60µA/amp
- $V_{OS}$ (max): 150µV
- $TCV_{OS}$: 1µV/°C
- Input bias current (max): 2nA
- -3dB bandwidth: 240kHz
- Rail-to-rail input and output
- Independent enable available
- -40°C to +125°C operation

NEW!!

Pb RoHS Compliant

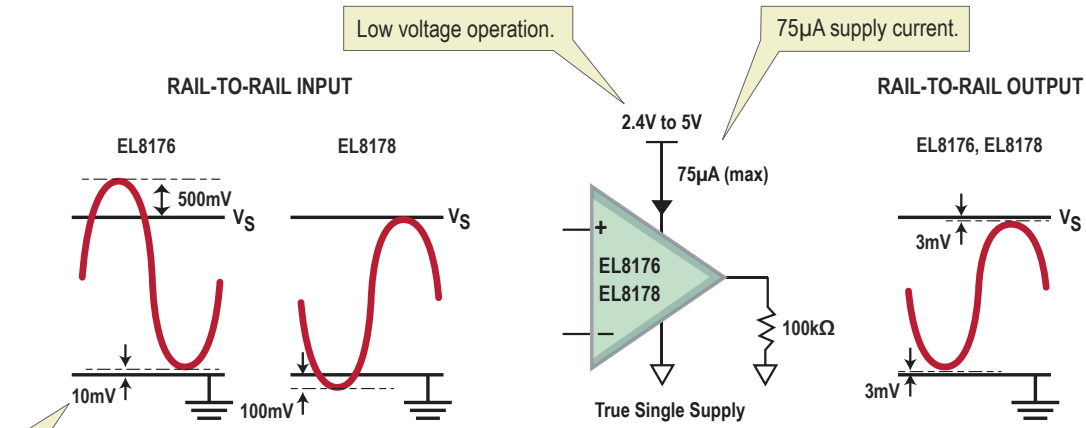
## Intersil's Precision Instrumentation Amplifier Family

| Part Number | Amp/Pkg | Input Stage | $V_{OS}$ (max) | $I_B$ (max) (nA) | Min. Gain (V/V) | GBW (kHz) | $I_{SS}$ (max) (µA/Amp) | Status | Package |
|---|---|---|---|---|---|---|---|---|---|
| EL8170 | Single | PNP | 250 | 2 | 100 | 600 | 78 | Released | 8 Ld SOIC |
| ISL28270 | Dual | PNP | 150 | 2 | 100 | 600 | 60 | Released | 16 Ld QSOP |
| ISL28470 | Quad | PNP | 150 | 2 | 100 | 600 | 60 | Sampling | 16 Ld QSOP |
| EL8172 | Single | PMOS | 300 | 0.2 | 100 | 600 | 78 | Released | 8 Ld SOIC |
| ISL28272* | Dual | PMOS | 300 | 0.2 | 100 | 600 | 78 | Sampling | 16 Ld QSOP |
| EL8173 | Single | PNP | 1000 | 2 | 10 | 600 | 78 | Released | 8 Ld SOIC |
| ISL28273* | Dual | PNP | 1000 | 2 | 10 | 600 | 78 | Sampling | 16 Ld QSOP |
| EL8171 | Single | PMOS | 1000 | 0.2 | 10 | 600 | 78 | Released | 8 Ld SOIC |

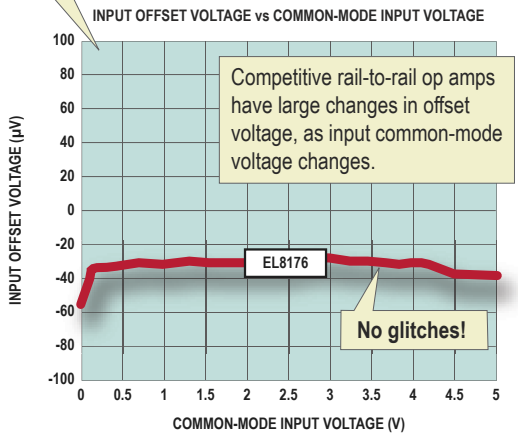
* Coming Soon

# Micropower Precision Op Amps Swing Rail-to-Rail without Input Offset Glitches

Intersil's EL817X delivers DC accuracy on just 75µA max of supply current.




Input swings rail-to-rail without offset glitches.




## Key Features

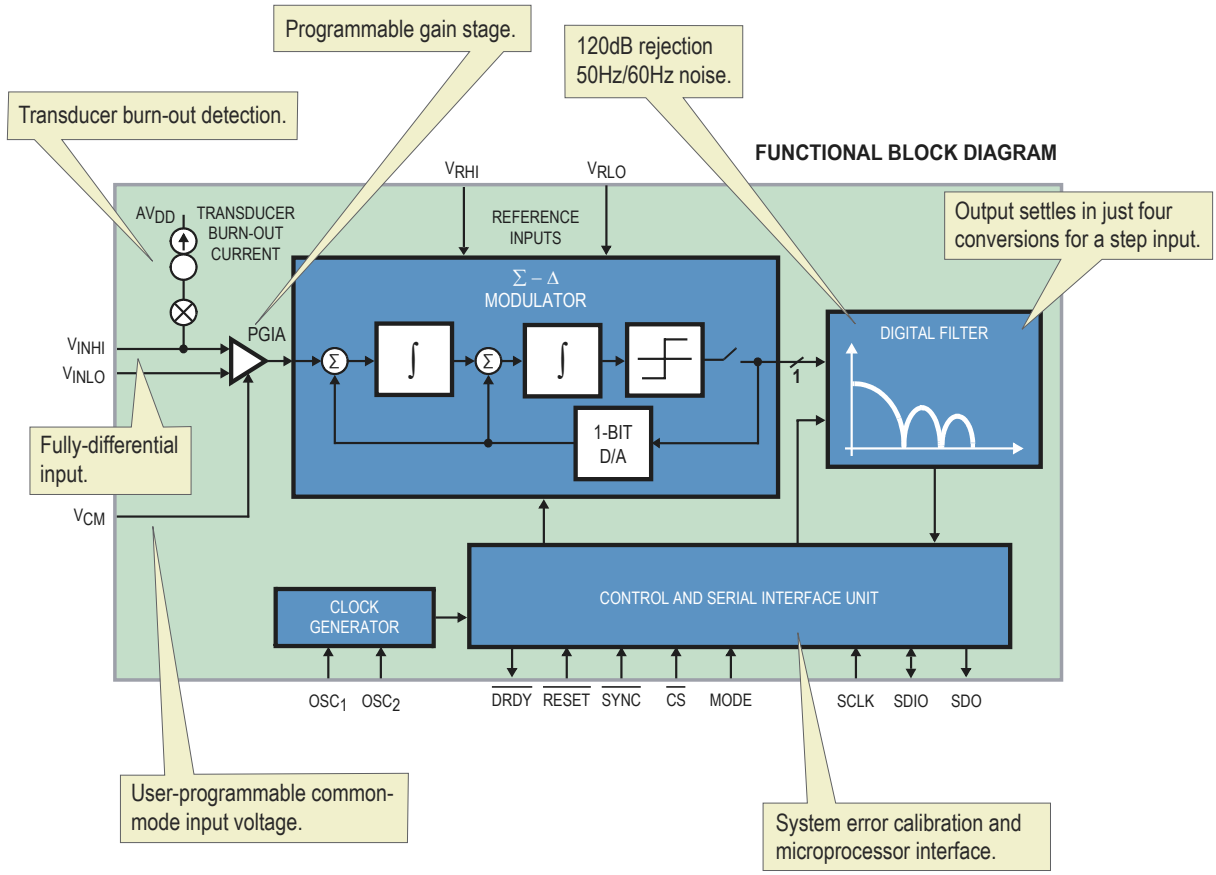
- Ultra-low 75µA (max) supply current
- Flat $V_{OS}$ over CMRR: 100µV (max)
- Single supply operation: 2.4V to 5V
- Low 15pA (max) (EL8178)
- Rail-to-rail input/output
- 26mA output drive
- 6 Ld SOT-23 and 8 Ld SOIC packages

## Intersil's Precision Amplifier Family

| Part Number | Amp/Pkg | Input Stage | $V_{OS}$ (max) (µV) | $I_B$ (max) (nA) | $TCV_{OS}$ (µV/°C) | GBW (kHz) | $I_{SS}$ (max) (µA/Amp) | Status | Package |
|---|---|---|---|---|---|---|---|---|---|
| EL8176 | Single | PNP | 100, 350 | 2 | 0.7 | 400 | 75 | Released | 6 Ld SOT-23, 8 Ld SOIC |
| ISL28276 | Dual | PNP | 100 | 2 | 0.3 | 400 | 75 | Released | 16 Ld QSOP |
| ISL28476 | Quad | PNP | 100 | 2 | 0.3 | 400 | 75 | Q406 | 16 Ld QSOP |
| ISL28286 | Dual | PNP | 600 | 3 | 1 | 400 | 75 | Sampling | 10 Ld MSOP |
| ISL28486 | Quad | PNP | 600 | 3 | 1 | 400 | 75 | Q406 | 16 Ld QSOP |
| EL8178 | Single | PMOS | 100, 400 | 0.05 | 1.1, 1.9 | 400 | 75 | Released | 6 Ld SOT-23, 8 Ld SOIC |
| ISL28278 | Dual | PMOS | 225 | 0.03 | 1.1 | 400 | 75 | Sampling | 16 Ld QSOP |
| ISL28478 | Quad | PMOS | 225 | 0.03 | 1.1 | 400 | 75 | Q406 | 16 Ld QSOP |
| EL8188 | Single | PMOS | 4000 | 0.075 | 1.1 | 250 | 75 | Released | 6 Ld SOT-23 |
| ISL28288 | Dual | PMOS | 2000 | 0.03 | 1.5 | 400 | 75 | Sampling | 10 Ld MSOP |
| ISL28488 | Quad | PMOS | 2000 | 0.03 | 1.5 | 400 | 75 | Sampling | 16 Ld QSOP |

# Flexible 24-bit Sigma Delta A/D Converter Delivers >130dB SNR

Intersil's HI7190 is a feature-rich 24-bit A/D converter, offering a unique combination of accuracy, low noise, and flexibility to help solve the issues associated with high resolution analog data capture.

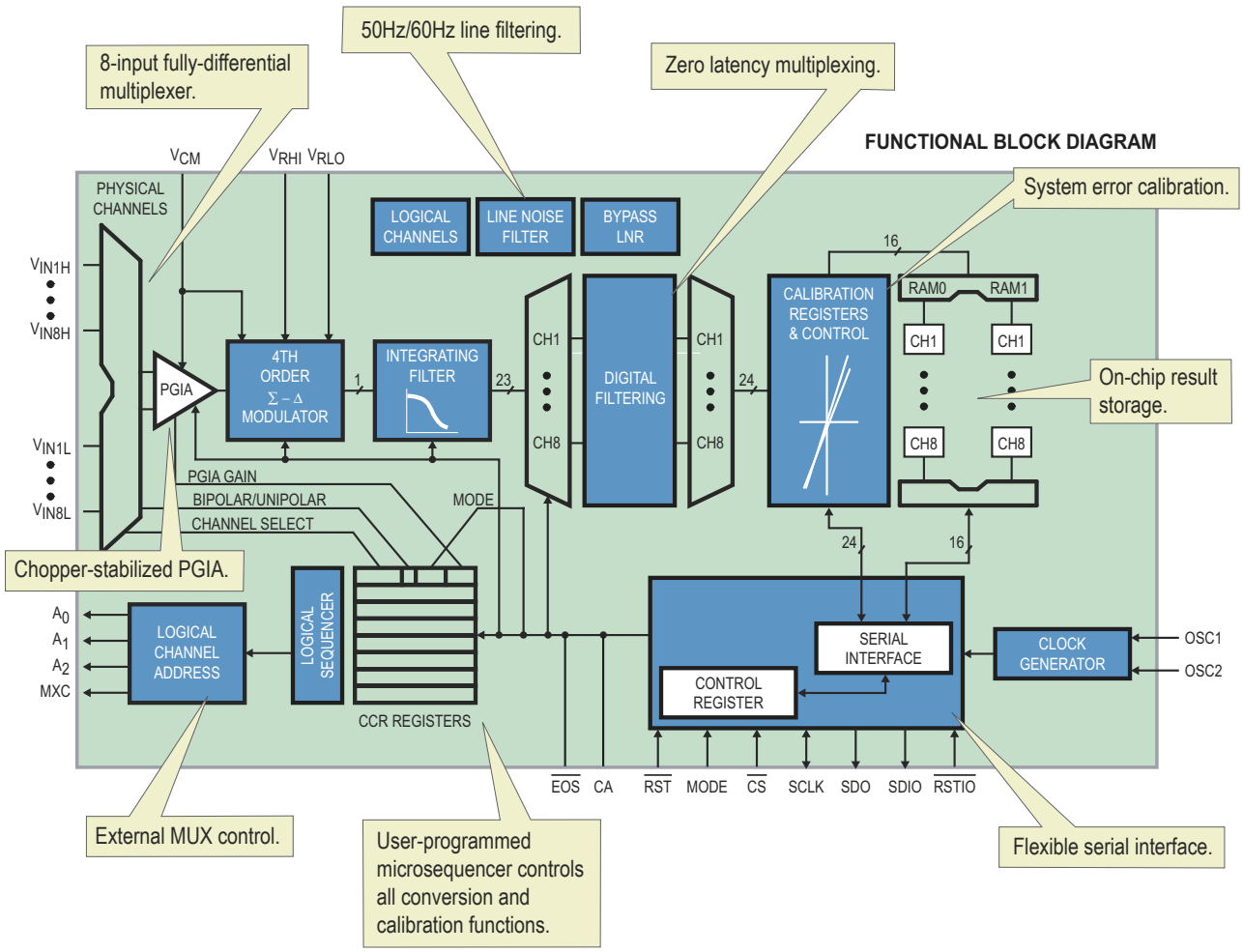



## Key Features

- 24-bit resolution
  - ±0.0007% INL
  - No missing codes to 22 bits
  - 130dB SNR (PGIA gain of 1)
- 50Hz/60Hz line noise suppression mode (120dB rejection when enabled)
- Flexible analog front end
  - Handles unipolar and bipolar input voltages
  - Programmable gain amplifier (gain settings form 1 to 128)
  - 20mV to ±2.5V full scale input range
- Low latency operation
  - Settles within four conversions
- Transducer burn-out detection
  - Current source to confirm sensor integrity before conversion
- System calibration capability
  - Allows user to digitally null system-wide zero and full-scale errors
- SPI interface
- 15mW power consumption

# 16-bit Sigma Delta Data Acquisition System Chip Offers Programmable Sequencing and Zero Latency Channel Switching

Intersil's HI7188 is an easy-to-use 8-channel, 16-bit A/D stand-alone subsystem that includes a unique blend of features, all integrated into a compact 44 Ld MQFP package.

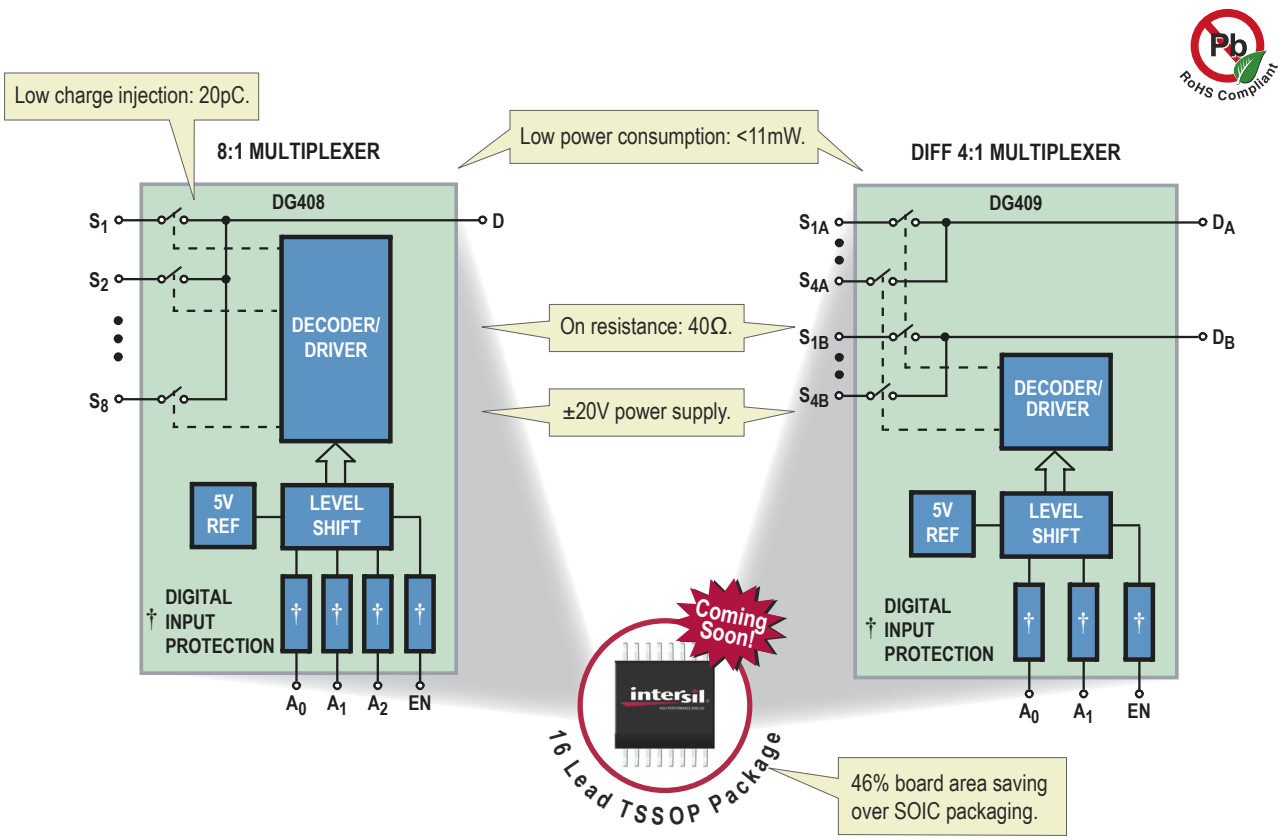



## Key Features

- 16-bit, 240 samples per second sigma delta A/D converter
  - ±0.0015% INL
  - Guaranteed no missing codes
- Powerful user-programmable microsequencer
  - Controlling all channel switching, filtering, and calibration functions
- Highly-programmable front end
  - Handles unipolar and bipolar input voltages
  - 8-channel differential input MUX
  - Chopper-stabilized programmable gain stage (gain options of 1, 2, 4, or 8)
  - Can control external MUXes via dedicated output pins
- Zero latency channel switching
- System calibration capability
  - Allows user to digitally null system-wide zero and full-scale errors
- On-chip results memory
  - Stores up to eight conversions
  - Burst mode result download via SPI interface
  - Two RAM banks to allow results to be read during next conversion cycle
- Full-scale and under-range detection
- 50Hz/60Hz line noise suppression mode (120dB rejection when enabled)
- 30mW power consumption

# Precision Analog Switches, MUXes, and Crosspoints

Intersil's DG family provides low on resistance, fast switching, high off isolation, and low leakage. Small footprint 16 Ld TSSOP and 16 Ld SOIC package significantly reduce board size in ±20V powered industrial applications.




## Single/Dual Supply High Voltage Switches

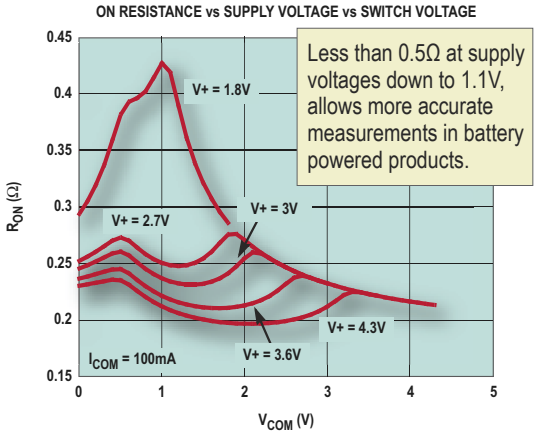
| Part Number | Configuration | Switches | Contacts | $R_{ON}$ @ ±13.5V (Ω) | Leakage Current (nA) | $T_{ON}$ / $T_{OFF}$ (ns) | Leakage (nA) | $V_{CC}$ Range (max) (V) |
|---|---|---|---|---|---|---|---|---|
| DG401 | SPST | 2 | NO | 20 | 0.04 | 110 / 60 | 0.01 | +5 to +34, ±5 to ±20 |
| DG403 | DPST | 2 | MIX | 20 | 0.04 | 110 / 60 | 0.01 | +5 to +34, ±5 to ±20 |
| DG411 | SPST | 4 | NC | 25 | 0.1 | 110 / 100 | 0.1 | +5 to +34, ±5 to ±20 |
| DG412 | SPST | 4 | NO | 25 | 0.1 | 110 / 100 | 0.1 | +5 to +34, ±5 to ±20 |
| DG413 | SPST | 4 | MIX | 25 | 0.1 | 110 / 100 | 0.1 | +5 to +34, ±5 to ±20 |
| DG441 | SPST | 4 | NC | 50 | 0.08 | 150 / 90 | 0.01 | +5 to +34, ±5 to ±20 |
| DG442 | SPST | 4 | NO | 50 | 0.08 | 150 / 110 | 0.01 | +5 to +34, ±5 to ±20 |
| DG444 | SPST | 4 | NC | 50 | 0.08 | 120 / 110 | 0.01 | +5 to +34, ±5 to ±20 |
| DG445 | SPST | 4 | NO | 50 | 0.08 | 120 / 160 | 0.01 | +5 to +34, ±5 to ±20 |

## Single/Dual Supply High Voltage Multiplexers

| Part Number | Configuration | Outputs | $R_{ON}$ @ ±10V (Ω) | Leakage Current (nA) | $T_{ON}$ / $T_{OFF}$ (ns) | Off Isolation dB @ kHz | $V_{CC}$ Range (max) (V) |
|---|---|---|---|---|---|---|---|
| DG406 | 16:1 | 1 | 50 | 0.04 | 150 / 70 | 69 / 100 | +5 to +34, ±5 to ±20 |
| DG407 | 8:1 | 2 (Diff) | 50 | 0.04 | 150 / 70 | 69 / 100 | +5 to +34, ±5 to ±20 |
| DG408 | 8:1 | 1 | 40 | 1 | 115 / 105 | 75 / 100 | +5 to +34, ±5 to ±20 |
| DG409 | 4:1 | 2 (Diff) | 40 | 1 | 115 / 105 | 75 / 100 | +5 to +34, ±5 to ±20 |

# Industry's Lowest Distortion and Highest ESD Sub 0.5Ω Analog Switches

9kV ESD-protected, +1.1V to +4.5V, single supply, dual SPDT switches ensure reliability in handheld applications.




## Low Voltage Precision Switches and MUXes

| Part Number | Configuration | $R_{ON}$ @ 2.7V (Ω) | $R_{ON}$ Flatness (Ω) | ESD (HBM) (kV) | Supply Voltages (V) | Packages |
|---|---|---|---|---|---|---|
| ISL84780 | Dual DPDT / Diff 2:1 MUX | 0.45 | 0.07 | 4 | 1.6 to 3.6 | 16 Ld TQFN, 16 Ld TSSOP |
| ISL8499 | Dual DPDT / Diff 2:1 MUX | 0.3 | 0.06 | 9 / 4 | 1.6 to 4.5 | 16 Ld QFN, 16 Ld TSSOP |
| ISL43L420 | Dual DPDT / Diff 2:1 MUX | 0.3 | 0.06 | 9 / 4 | 1.1 to 4.5 | 16 Ld QFN |
| ISL84781 | 8:1 MUX | 0.41 | 0.056 | 4 | 1.6 to 3.6 | 16 Ld TQFN, 16 Ld TSSOP |
| ISL84782 | Diff 4:1 MUX | 0.5 | 0.056 | 4 | 1.6 to 3.6 | 16 Ld TQFN, 16 Ld TSSOP |
| ISL43L840 | Dual 4:1 MUX | 0.5 | 0.056 | 4 | 1.6 to 3.6 | 16 Ld QFN, 16 Ld TSSOP |

## High Voltage Precision Multiplexers

| Part Number | Configuration | Outputs | $R_{ON}$ @ ±15V (Ω) | Leakage Current (nA) | $T_{ON}$ / $T_{OFF}$ (ns) | Off Isolation dB @ kHz | $V_{CC}$ Range (V) |
|---|---|---|---|---|---|---|---|
| HI-524 | 4:1 | 1 | 700 | 0.7 | 180 / 180 | 65 / 10,000 | ±15 |
| HI-509 | 4:1 | 2 (Diff) | 180 | 0.3 | 250 / 250 | 68 / 100 | ±15 |
| HI-1828A | 4:1 | 2 (Diff) | 250 | 250 (max) | 300 / 300 | - | ±15 |
| HI-518 | 4:1 | 2 (Diff / Dual) | 480 | 0.015 | 120 / 140 | 45 / 500 | ±15 |
| HI-539 | 4:1 | 2 (Diff) | 650 | 0.15 | 250 / 160 | 124 / 1 | ±5 to ±18 |
| HI-508 | 8:1 | 1 | 180 | 0.3 | 250 / 250 | 68 / 100 | ±15 |
| HI-1818A | 8:1 | 1 | 250 | 250 (max) | 300 / 300 | - | ±15 |
| HI-518 | 8:1 | 1 | 480 | 0.015 | 120 / 140 | 45 / 500 | ±15 |
| HI-507 | 8:1 | 2 (Diff) | 180 | 0.3 | 250 / 250 | 68 / 100 | ±15 |
| HI-516 | 8:1 | 2 (Diff / Dual) | 620 | 0.04 | 120 / 140 | 55 / 500 (min) | ±15 |
| HI-516 | 16:1 | 1 | 620 | 0.04 | 120 / 140 | 55 / 500 (min) | ±15 |
| HI-506 | 16:1 | 1 | 180 | 0.3 | 250 / 250 | 68 / 100 | ±15 |

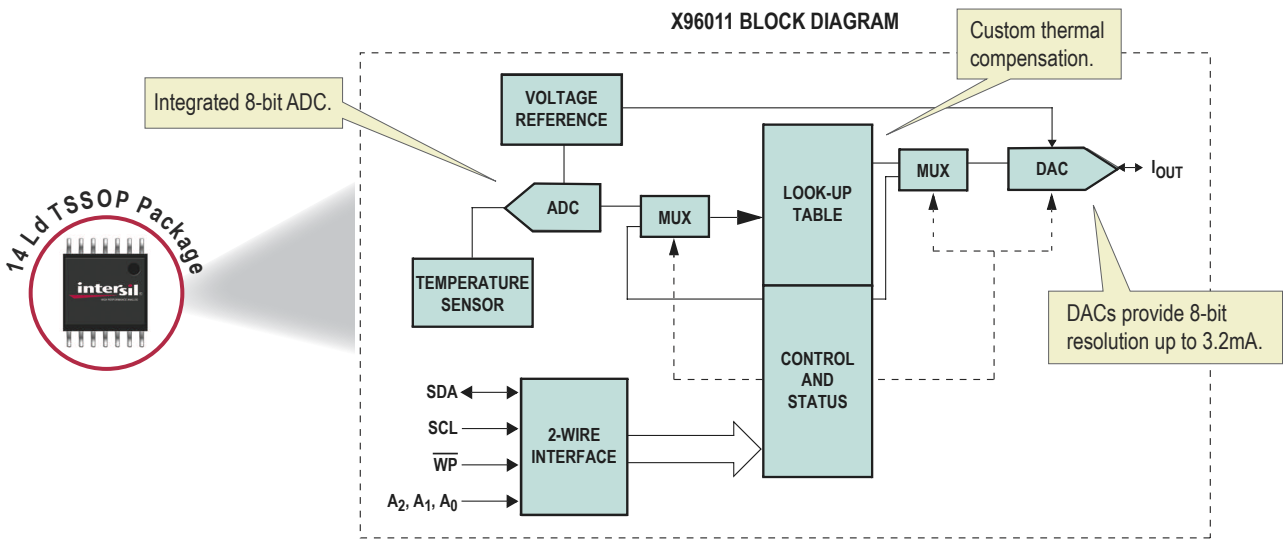
## Over-Voltage Protected Precision Multiplexers

| Part Number | Configuration | Outputs | Input Over-Voltage Range ($V_{PP}$) | $R_{ON}$ @ ±15V (Ω) | Leakage Current (nA) | $T_{ON}$ / $T_{OFF}$ (ns) | Off Isolation dB @ kHz | $V_{CC}$ Range (max) (V) |
|---|---|---|---|---|---|---|---|---|
| HI-546 | 16:1 | 1 | 70 | 1500 | 0.1 | 300 / 300 | 68 / 100 | ±5 to ±20 |
| HI-506A | 16:1 | 1 | 70 | 1500 | 0.1 | 300 / 300 | 68 / 100 | ±5 to ±20 |
| HI-548 | 8:1 | 1 | 70 | 1500 | 0.1 | 300 / 300 | 68 / 100 | ±5 to ±20 |
| HI-508A | 8:1 | 1 | 70 | 1500 | 0.1 | 300 / 300 | 68 / 100 | ±5 to ±20 |
| HI-547 | 8:1 | 2 (Diff) | 70 | 1200 | 0.1 | 300 / 300 | 68 / 100 | ±5 to ±20 |
| HI-507A | 8:1 | 2 (Diff) | 70 | 1500 | 0.1 | 300 / 300 | 68 / 100 | ±5 to ±20 |
| HI-549 | 4:1 | 2 (Diff) | 70 | 1500 | 0.1 | 300 / 300 | 68 / 100 | ±5 to ±18 |
| HI-509A | 4:1 | 2 (Diff) | 70 | 1500 | 0.1 | 300 / 300 | 68 / 100 | ±5 to ±20 |

# Programmable Current Sources Offer Temperature Compensation and Maintain Constant Bias Over Temperature

Intersil's X96010, X96011, and X96012 combine digitally controlled programmable current generator(s) and temperature compensation with dedicated look-up tables.

RoHS Compliant




## Key Features

- $V_{DD}$: 3V to 5.5V
- Temp sensor-accuracy for system diagnostics: 0.55°C per step (-40°C to +100°C range)
- Programmable current generator: ±1.6mA/Ch
  - Resolution: 8-bit (256-step)
- ADC: Assures accuracy with the external $V_{SENSE}$
- DAC: Good linearity needed for bias applications
  - INL: ±1 LSB
  - DNL: ±0.05 LSB
- Precision voltage reference : ±0.4% @ +25°C, ±100ppm/°C drift
- Available in 14 Ld TSSOP package

## Applications

- PIN diode bias control
- RF PA bias control
- Laser diode bias control
- Sensor signal conditioning
- Open loop temp compensation

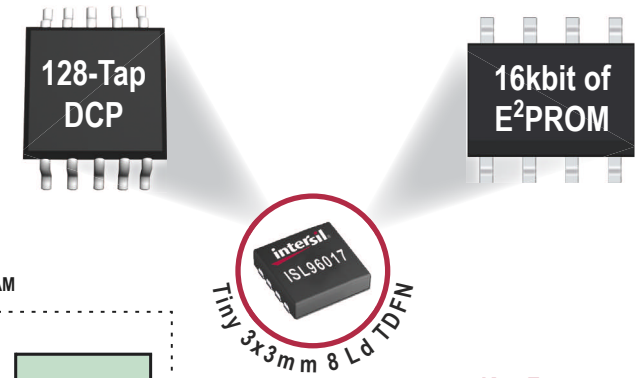
## Key Parameters

| Device | Title | Features/Functions | | | | | | | Package |
|---|---|---|---|---|---|---|---|---|---|
| | | Internal Temperature Sensor | External Sensor Input | $V_{REF}$ Input/ Output | General Purpose EEPROM | Look-Up Table Organization | # of Current Output DACs | DAC Full Scale Control | |
| X96010 | Sensor Conditioner with Dual Look Up Table Memory and DACs | No | Yes | Yes | No | Dual Bank | Dual | Ext | 14 Ld TSSOP |
| X96011 | Temperature Sensor with Single Look Up Table Memory and DAC | Yes | No | No | No | Single Bank | Single | Int | 14 Ld TSSOP |
| X96012 | Universal Sensor Conditioner with Dual Look Up Table and DACs | Yes | Yes | Yes | Yes | Dual Bank | Dual | Ext/Int | 14 Ld TSSOP |

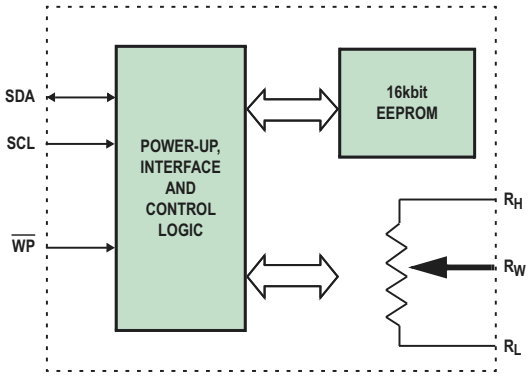
Ext = External, Int = Internal

# Optimize Space with Integrated 128-Tap Non-Volatile DCP and 16kbit E²PROM

Intersil's ISL96017, powered from a single 3.3V supply, integrates a 128-tap non-volatile DCP, 16kbit E²PROM, and a 2-wire I²C serial interface.




BLOCK DIAGRAM

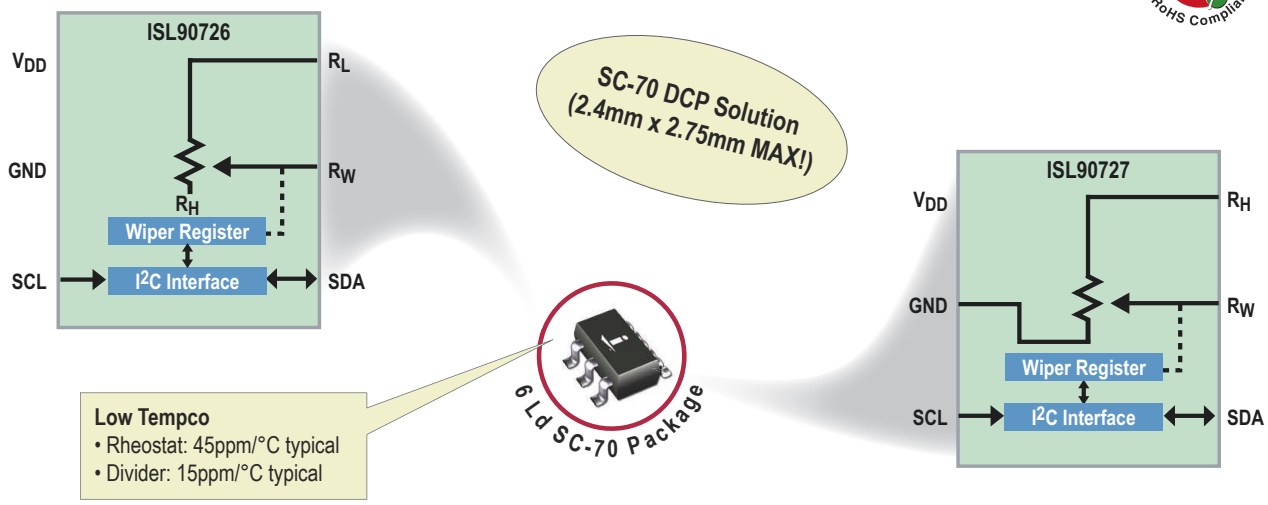



**Key Features**

- General purpose EEPROM memory: 16kbit
- Low standby current: 10µA
- Wiper resistance: 100Ω
- Temperature range: -40°C to +85°C

# 128-Tap Single Supply Volatile DCP Solution in SC-70 Package

Intersil's ISL90726 and ISL90727 in 6 Ld SC-70 are ideal choices for smaller handheld applications.



# Intersil: The Leader in Digital Potentiometers

## Non-Volatile

- **Single 16-Tap**
  - X9116 - 10kΩ, Up-Down
- **Single 32-Tap**
  - [D] X9313 - 1kΩ / 10kΩ / 50kΩ, Up-Down
  - [D] X9314 - 10kΩ, Log Taper, Up-Down
  - X9315 - 10kΩ / 50kΩ / 100kΩ, Up-Down
  - X93154 - 50kΩ, Up-Down, 2-Terminal
  - X93155 - 50kΩ, Up-Down, 2-Terminal
  - X93156 - 12.5kΩ / 50kΩ, Up-Down
  - [D] X9511 - 1kΩ / 10kΩ, Push Button
- **Single 64-Tap**
  - X9429 - 2.5kΩ / 10kΩ, 2-Wire
- **Single 100-Tap**
  - X9317 - 1kΩ / 10kΩ / 50kΩ / 100kΩ, Up-Down
  - [E] X9318 - 10kΩ, Up-Down
  - [E] X9319 - 10kΩ / 50kΩ / 100kΩ, Up-Down
  - [D] X9C102 - 1kΩ, Up-Down
  - [D] X9C103 - 10kΩ, Up-Down
  - [D] X9C104 - 100kΩ, Up-Down
  - [D] X9C503 - 50kΩ, Up-Down
  - [D] X9C303 - 32kΩ, Log Taper, Up-Down
- **Single 128-Tap**
  - ISL22316 - 10kΩ / 50kΩ, $I^2C$
  - ISL22319 - 10kΩ / 50kΩ, $I^2C$, Wiper Only
  - [E] ISL95311 - 10kΩ / 50kΩ, $I^2C$
  - [D] ISL95711 - 10kΩ / 50kΩ, $I^2C$
  - ISL96017 - 10kΩ / 50kΩ, $I^2C$ (16kbits extra EEPROM)
  - ISL22416 - 10kΩ / 50kΩ, SPI
  - ISL22419 - 10kΩ / 50kΩ, SPI, Wiper Only
  - [E] ISL95310 - 10kΩ / 50kΩ, Up-Down
  - [D] ISL95710 - 10kΩ / 50kΩ, Up-Down
- **Single 256-Tap**
  - ISL95810 - 10kΩ / 50kΩ, $I^2C$
- **Single 1024-Tap**
  - [D] X9110 - 100kΩ, SPI
  - X9111 - 100kΩ, SPI
  - [D] X9118 - 100kΩ, 2-Wire
  - X9119 - 100kΩ, 2-Wire
- **Dual 32-Tap**
  - X93254 - 50kΩ, Up-Down, 2-Terminal
  - X93255 - 50kΩ, Up-Down, 2-Terminal
  - X93256 - 50kΩ, Up-Down
- **Dual 64-Tap**
  - [D] X9410 - 10kΩ, SPI
  - [D] X9221A - 2kΩ / 10kΩ / 50kΩ, 2-Wire
  - [D] X9418 - 2.5kΩ / 10kΩ, 2-Wire
- **Dual 128-Tap**
  - ISL22326 - 10kΩ / 50kΩ, $I^2C$
  - ISL22329 - 10kΩ / 50kΩ, $I^2C$, Wiper Only
  - ISL22426 - 10kΩ / 50kΩ, SPI
  - ISL22429 - 10kΩ / 50kΩ, SPI, Wiper Only
- **Dual 256-Tap**
  - X95820 - 10kΩ / 50kΩ, $I^2C$
  - [D] X9260 - 50kΩ / 100kΩ, SPI
  - X9261 - 50kΩ / 100kΩ, SPI
  - [D] X9268 - 50kΩ / 100kΩ, 2-Wire
- **Quad 64-Tap**
  - [D] X9400 - 2.5kΩ / 10kΩ, SPI
  - X9401 - 10kΩ, SPI
  - [D] X9241A - 2kΩ / 10kΩ / 50kΩ, 2-Wire
  - [D] X9408 - 2.5kΩ / 10kΩ, 2-Wire
  - X9409 - 2.5kΩ / 10kΩ, 2-Wire
- **Quad 128-Tap**
  - ISL22346 - 10kΩ / 50kΩ, $I^2C$
  - ISL22349 - 10kΩ / 50kΩ, $I^2C$, Wiper Only
  - ISL22446 - 10kΩ / 50kΩ, SPI
  - ISL22449 - 10kΩ / 50kΩ, SPI, Wiper Only
- **Quad 256-Tap**
  - X95840 - 10kΩ / 50kΩ, $I^2C$
  - [D] X9250 - 50kΩ / 100kΩ, SPI
  - X9251 - 50kΩ / 100kΩ, SPI
  - X9252 - 2kΩ / 10kΩ / 50kΩ / 100kΩ, 2-Wire
  - [D] X9258 - 50kΩ / 100kΩ, 2-Wire
  - X9259 - 50kΩ / 100kΩ, 2-Wire

## Special Function DCPs

- **TFT/LCD Programmable $V_{COM}$ Calibrator (128 Step)**
  - ISL45041 - $I^2C$
  - ISL45042 - Up-Down
- **Triple Multi-Tap DCP with 2kbits General Purpose $E^2$PROM**
  - X9520 - 64-Tap / 10kΩ, 100-Tap / 10kΩ, 256-Tap / 100kΩ, 2-Wire
- **Single 128-Tap DCP with 16kbits General Purpose $E^2$PROM**
  - ISL96017 - 10kΩ / 50kΩ, $I^2C$
- **Sensor Conditioners with Look-Up Tables, Memory's DACs**
  - X96010 - Dual, 2-Wire
  - X96011 - Single with Temperature Sensor, 2-Wire
  - X96012 - Dual with Temperature Sensor, 2-Wire
- **Micropower Programmable Voltage Reference**
  - X60250

## Volatile

- **Single 32-Tap**
  - X9015 - 10kΩ / 50kΩ / 100kΩ, Up-Down
  - ISL90460 - 10kΩ / 50kΩ / 100kΩ, Up-Down, Rheostat
  - ISL90461 - 10kΩ / 50kΩ / 100kΩ, Up-Down, 2-Terminal
  - ISL90462 - 10kΩ / 50kΩ / 100kΩ, Up-Down, 2-Terminal
- **Single 128-Tap**
  - ISL90726 - 10kΩ / 50kΩ, $I^2C$, 2-Terminal
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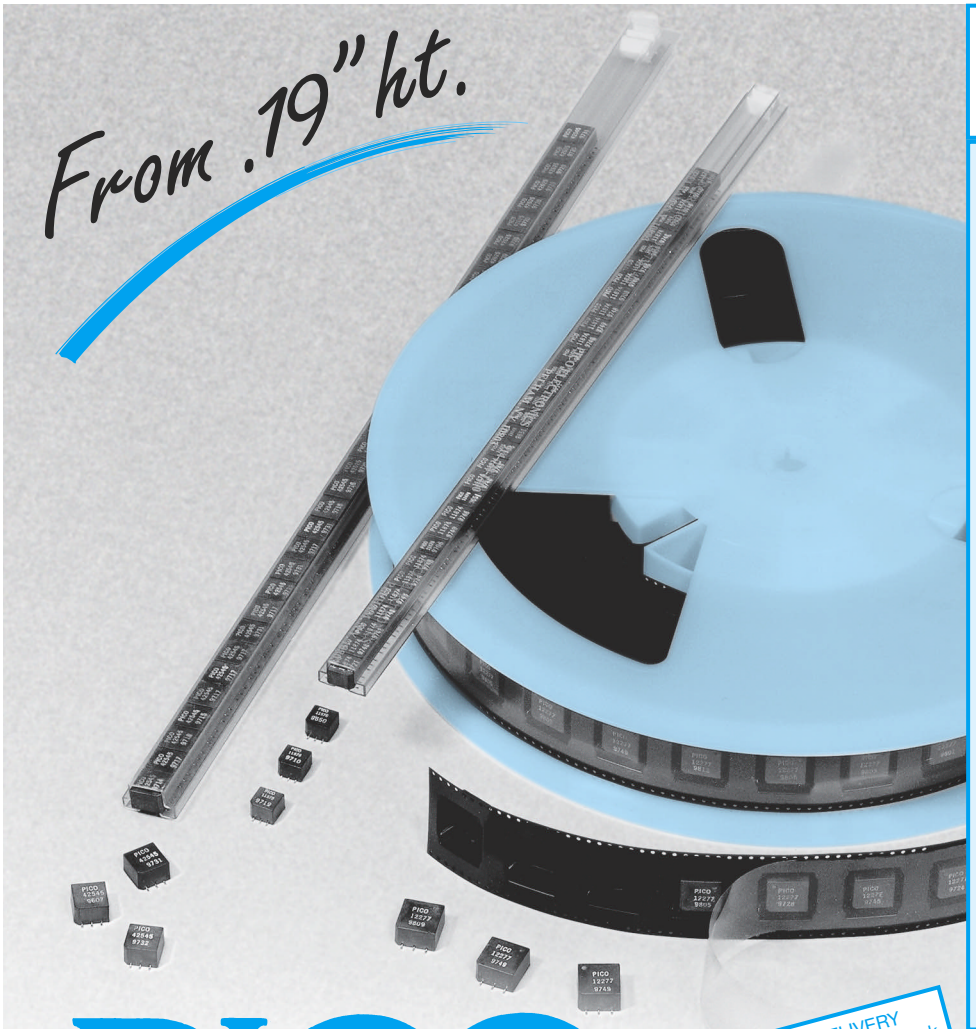


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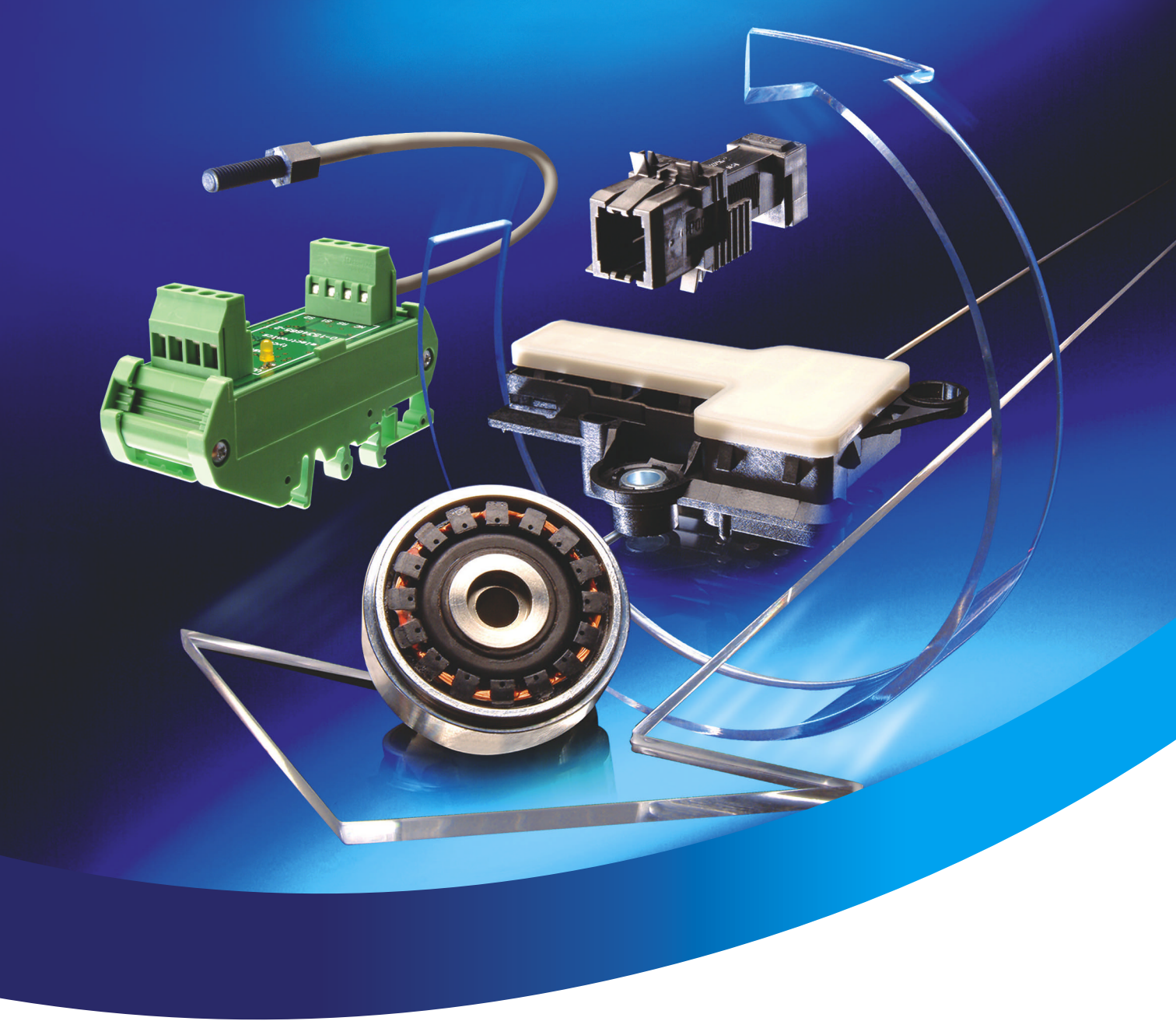

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# Formal techniques solidify power-grid verification

FORMAL GRID VERIFICATION PROVIDES AN EARLY CHECKPOINT IN THE DESIGN FLOW, DURING WHICH A USER CAN SIGN OFF ON THE STRUCTURAL INTEGRITY OF THE POWER GRID BEFORE PROCEEDING TO VOLTAGE-DROP AND ELECTROMIGRATION ANALYSIS.

The number of components that SOCs (systems on chips) use is increasing dramatically as designs move into 90/65-nm technologies. Ensuring proper delivery of power to all the components is becoming more difficult. Designers must prevent functional and performance problems that time-varying drops in the voltage supplied to the components induce. The number and runtime of voltage-drop simulations and the amount of data to look at increases. Structural artifacts in the power grid, such as highly resistive connections due to cutout metal, are visible only after these costly simulations, which you need to repeat once you fix the artifacts, leading to unnecessary iterations. Finding localized problems gets even harder as the amount of data to debug increases with chip complexity.

Designers can employ a new technology to sign off on the structural integrity of the power grid early on, before proceeding with any power-consumption, voltage-drop, or electromigration simulations. The technique is similar to formal verification, which proves assertions independently of vector stimulus.

## VOLTAGE-DROP FAILURES

**Table 1** gives some examples of recent power-distribution-related failures. The first major questions for power-management engineers to ask are: Do power pins of all hard macros, such as RAMs, connect properly to the power grid? Do power pins of all standard cells connect properly to the power grid? Are there any defects in the power-grid geometries? These concerns grow with each new design, because new designs typically have more hard macros, more standard cells, and more polygons that make up the power grid. Because these problems directly affect the voltage-drop- and electromigration-analysis results, such analyses are not valid until you solve the problems.

During the floorplanning stage, engineers—or their dutiful scripts—lay out power rings and grids, cut out certain parts of the network to accommodate hard macros, taper the grid segments to open up routing resources, and do various other tricks. Sometimes, they design certain parts of the network to establish connection by abutment. Finally, they must verify all of these maneuvers against the three aforementioned design questions. Here are a few real-life scenarios arising from perfectly valid manipulations of the layout that cause concerns:

- Two physical partitions abut in the top level, but the power grid that is supposed to run across the partition boundaries has an open circuit.
- A partition owner cuts out a sizable chunk of power grid to open routing resources.
- Vias are missing from where they are supposed to be.
- A long power rail connects to a power trunk from one end only, because a hard macro blocks out the other end (**Figure 1**).
- The hard-macro locations shift in the floorplan, or the latest LEF (library-exchange-format) file from the IP (intellectual-property) vendor differs from its previous version.
- Someone or a bug-constrained script removes a power trunk.

## A TOOLBOX FOR POWER-GRID ANALYSIS

Most place-and-route tools can verify whether a given instance connects to the power grid. However, a mere connection is not necessarily a proper connection all the way back to the power supply. Analysis that you do not base on resistance can't verify whether a connection is electrically sound.

You normally answer the three design questions by using traditional voltage-drop-analysis tools in a manner different from the one for which they were designed: to do sanity-check simulations rather than to determine whether voltage-drop values are within specification in functions and timing.

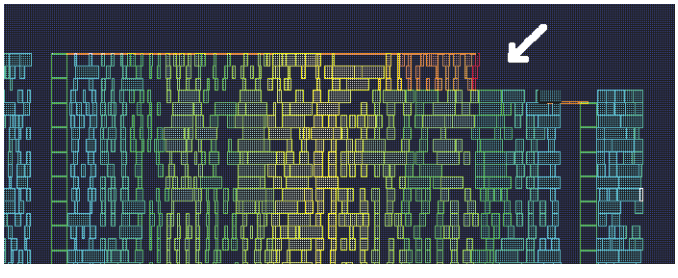

Figure 1 The top three rows of instances connect to power rails supplied by one end only—the power trunk on the left.

For this purpose, you use static voltage-drop analysis or, less often, vectorless dynamic analysis, instead of vector-based dynamic analysis, to ensure stimulation of all areas of the design. Although these events are full-blown voltage-drop simulations, the accuracy of the voltage-drop values is irrelevant, because these events are only sanity checks. Engineers at this stage are focusing on finding structural problems in the power grid. For example, a black region in the color-coded voltage-drop map is a potentially unconnected instance. If visually zooming around a hard macro in the map shows sudden color changes, there is a good chance the power pins are connected in a highly resistive manner (**Figure 2**) or not connected at all.

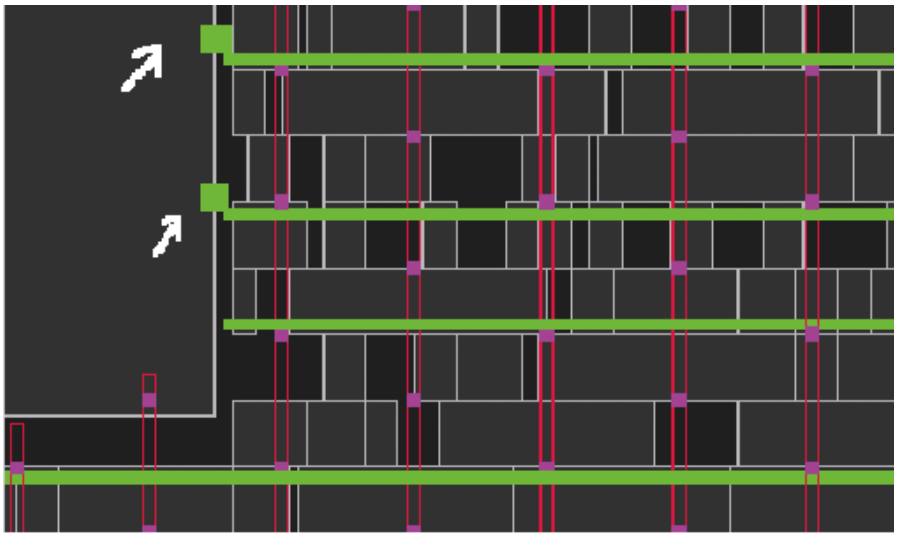

Figure 2 The two pins on the right side of the hard macro barely touch the power rails, resulting in highly resistive connections.

This method is tedious and, hence, error-prone and does not guarantee full coverage, because an engineer may miss a localized spot in the design. How do you see one 1-pixel-wide red or black area in the voltage-drop map? You could zoom in, but unless you zoom around the whole design, there would always be a chance that you would miss that spot. The process gets more impractical as the number of components in the design increases. What's more, you have to repeat this whole analysis when the floorplan or the power distribution changes.

A not-so-typical method, yet a better one for this purpose, is to perform differential voltage-drop analysis (dV/dx)—the same voltage-drop-analysis simulation, but in a different way. In this method, the engineer writes a script to postprocess the raw voltage-drop results exiting from the tool and calculates voltage differences (dV) at neighboring data points (dx) (**Figure 3**). Because voltage drops gradually in a well-connected network, the dV/dx should be small. The data points at which the dV/dx is large are potential locations of highly resistive connections, indicating structural problems.

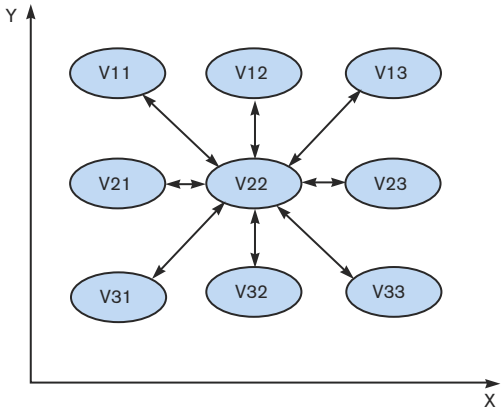


Figure 3 This method compares the voltage of a data point (V22) with its topological neighbors along the X and Y dimensions of the design.

Basically, the script looks at each data point, finds the differences with its neighbors, and reports the results in a file that first lists the data points that see the largest voltage differences. In a sense, the script does the tedious task of looking at each part of the design—much faster than a person can do it and as quickly and as often as necessary. Using this report, an engineer can focus his time on the problematic locations.


Figure 4 The value of dx can be large when you base dV/dx on instance power pins.

## FINDING LOCALIZED DEFECTS

This method is especially useful in pinpointing localized defects. In a conventional voltage-drop map, such defects show up as little red dots that are virtually impossible to spot. (Zooming helps but only if you know you need to zoom to that location.) Because these spots create large voltage differences from their neighbors, they show up loud and clear at the top of the dV/dx reports. Similarly, even if the absolute

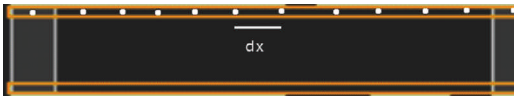


Figure 5 The value of dx is more granular when you base dV/dx on extraction nodes.


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value of voltage drop is too low to warrant a red mark in the voltage-drop results, a high difference from the neighbor's value indicates a problem that dV/dx analysis would catch.

You can perform this analysis in at least two ways, depending on where you base the data points in the voltage-drop simulation. You can base them on either the instance pin or the parasitic-extraction node using SPEF (Standard Parasitic Exchange Format) nodes. Voltage-drop values per instance pin are more readily available from conventional voltage-drop-analysis tools, making the first method easier for a design engineer to implement. However, in this method, the minimum distance between data points (dx) is the distance between instance pins, which may be large. For example, an open circuit at a power rail between two neighboring standard cells (**Figure 4**) causes high dV/dx for pins of each of the cells, and locating the problem requires inspection of the entire distance between them. If cells are not close to each other, dx can be a relatively long piece of power rail to inspect, compared with the second method.

In the parasitic-extraction-node-based dV/dx analysis (**Figure 5**), dx is much smaller, because it is merely the distance between two parasitic nodes. Hence, it can better pinpoint local problems. For example, it can get you directly to the location of an open circuit in a power rail. However, external implementation of this method is not trivial. Therefore, it should be a built-in feature of the voltage-drop-analysis tool.

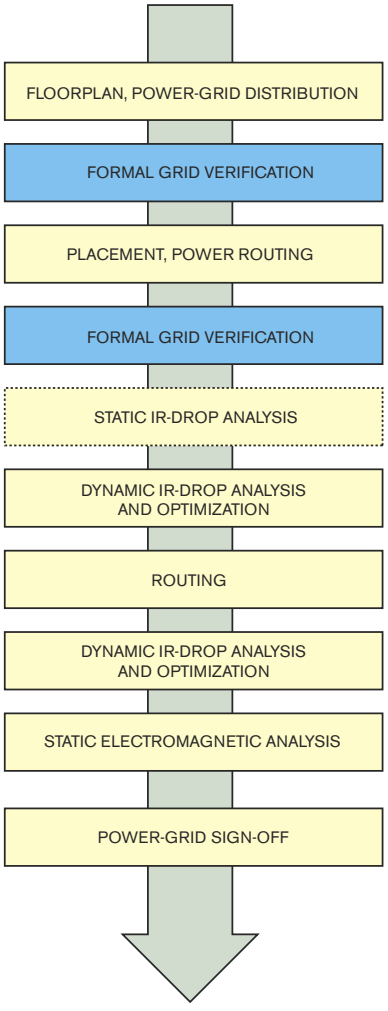


Figure 6 Formal grid verification is analogous to formal verification of logic functions.

These methods use full-blown voltage-drop simulations to find structural defects, unnecessarily moving the detection and prevention of such defects to later stages in the design cycle. Ideally, any kind of verification should occur as early and as often as possible. Moreover, these simulations are costly in runtime, memory footprint, and licensing fees. In addition, engineers must perform other steps, such as tedious debugging or developing postprocessing scripts.

You can answer the three aforementioned questions earlier in the design cycle without running these costly, late-stage simulations in a more practical manner and with faster turnaround times by instead employing formal grid verification.

## A FORMAL APPROACH

Formal grid verification is analogous to formal verification of logic functions. It is vector-independent and hence provides full coverage of the power grid. Rather than relying on vectors, a tool tests provable assertions. When it disproves an assertion, the tool can generate a trace-back that shows how the assertion is violated. **Figure 6** shows how formal power-grid verification fits into a power-grid-sign-off flow.

As soon as a designer lays out the power-grid distribution and places the hard macros at the floorplan stage, the tool formally identifies the defects at the distribution network and the problems at the connectivity of hard macros. Similarly, when standard-cell placement and power routing are complete, the tool can formally verify their proper connectivity.

One example of a provable assertion that you can use for formal grid verification is a limit on the effective resistance, $R_{EFF}$, of the path from any instance pin back to a supply. This assertion verifies electrical and physical connectivity. Analysis you base on such an assertion finds paths with poor connectivity or lack of connectivity.

In other words, a pin with higher than expected $R_{EFF}$ indicates a potential connectivity problem; so does a pin with higher $R_{EFF}$ than its neighboring pins. A pin with no calculable $R_{EFF}$ indicates an open circuit along the path to supply, which causes no alternative routes into which the the current could detour, such as a hard-macro pin that does not connect to the power rail.

For example, a missing via causes current to detour to instance pins through more resistive paths. Similarly, two

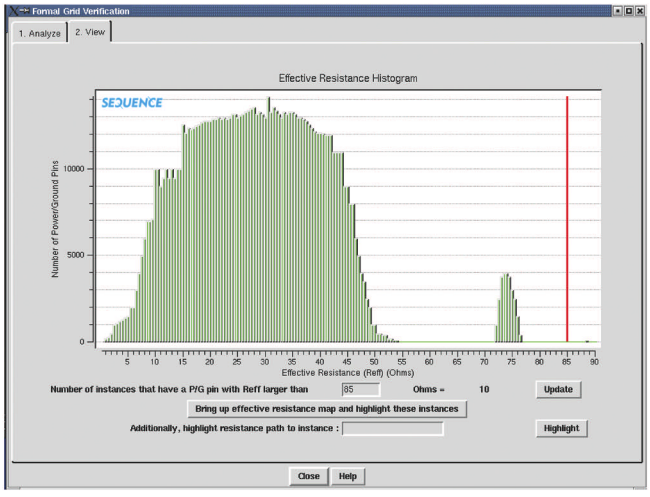


Figure 7 One way to visualize the pins is to create an effective resistance histogram.

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pieces of power rail that don't abut each other cause an open circuit at that point, and current takes a more resistive path to reach the destination. Hence, if there is a way to obtain $R_{EFF}$ for each power pin in the design, then there is a way to earlier detect power-grid-integrity problems.

In a small circuit, you can easily measure the resistance from a point inside the power grid back to the supply by converting series and parallel resistors into a single $R_{EFF}$. There are matrix techniques to get the $R_{EFF}$ of a mesh-connected grid containing millions of resistors. Another way to find this resistance is to use any vendor's static-voltage-drop tool and insert only one current source at the instance of interest. The result has its peak-voltage drop at the current source, with a gradual change down to zero voltage drop at the supply points. Given this peak-voltage drop ($I \times R_{EFF}$), you obtain the $R_{EFF}$ by a single multiplication. You can set the current source (I) to a unit current—for example, 1 µA—to further simplify the calculation.

But performing one full static solution for each instance in the design is not computationally practical. Even if a static solution took only a minute for a million-instance design, at least two million such static solutions would be necessary—one for power pins and one for ground—adding up to *four years* of runtime.

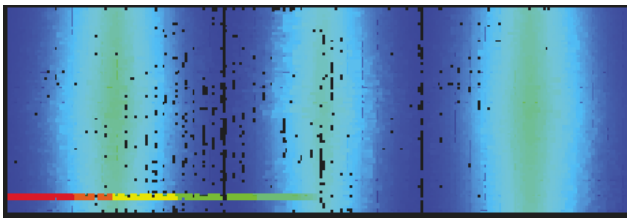

Figure 8 A familiar way to visualize the results is with a color-coded map of effective resistance.

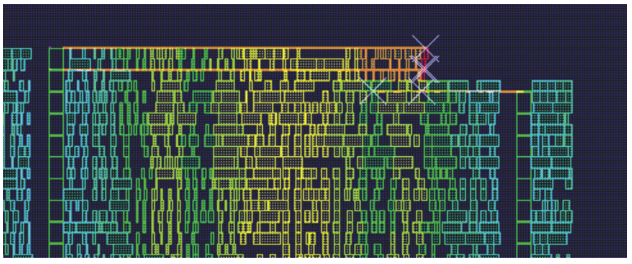

Figure 9 In formal verification, a trace-back should accompany any violation of an assertion, in which the tool generates information the designer can use to inspect the problem.

## A PRACTICAL WAY TO MEASURE $R_{EFF}$

There is a way to practically compute $R_{EFF}$ values. It involves tracing the parasitic resistors on the path to a destination-instance power pin from a supply tap. You obtain the resistor values from parasitic extraction of the power grid—for example, a power-grid SPEF file. You can perform tracing by means of a graph-walking algorithm that goes from node to node in the extracted-resistance-node matrix and stores the minimum resistance on each path. You then simply add the resistances along the least resistive path to yield $R_{EFF}$.

The power-supply taps attach to an initial power-distribution network—for example, a mesh made of top metal layers—typically yielding many paths through which current can travel. Sequence Design's (www.sequencedesign.com) formal-grid-verification tool CoolCheck employs the patent-pending REDUX (resistive-node-edge-detection-using-parasitic-extraction) algorithm to reduce the number of paths to trace. Using this method, tracing runtime and memory footprint is much smaller than in full-blown voltage-drop analysis.

Once you obtain the $R_{EFF}$ results, there are several ways of visualizing them. One way is to create a histogram of the $R_{EFF}$ for the pins (**Figure 7**). The horizontal axis represents $R_{EFF}$

TABLE 1 POWER-DISTRIBUTION-RELATED FAILURES

| Application | Failure | Cost |
|---|---|---|
| 90-nm networking flip-chip | High peak current in scan mode | Four months of debugging time on silicon and re-spin |
| 90-nm set-top-box, flip-chip | Mutual inductance on I/O | Three to four months of debugging, scaled power grid, and re-spin |
| 90-nm networking flip-chip | I/O buffers away from bumps had peak-voltage drop | Painful Spice simulations to debug and re-spin |
| 130-nm broadband-DSL flip-chip | High peak current in scan mode | Re-spin |
| 130-nm networking flip-chip | Poor decoupling-capacitance density around memory-control logic | Six- to nine-month delay (had to go from ASIC vendor to in-house design) |
| 130-nm PCI-bridge wire bond | Excessive clock jitter as a result of peak-voltage drop | Re-spin |
| 130-nm Bluetooth wire bond | High peak current in test mode | Part shipped with incomplete test; fix in re-spin |
| 130-nm consumer-electronics wire bond | High peak current around scan flops | Re-spin |

values in ohms. The vertical axis represents the number of pins with the corresponding $R_{EFF}$.

This histogram is, in a sense, the $R_{EFF}$ signature of the design. In this example, it indicates that most of the power pins in the design have $R_{EFF}$ of less than 50Ω. Hence, any pin with $R_{EFF}$ relatively larger than 50Ω is suspect for potential connectivity problems.

In this case, there are 10 instances in which power pins have $R_{EFF}$ larger than 85Ω. The red line represents the location of this resistance value in the histogram. It clearly shows that this value is outside the $R_{EFF}$ that the rest of the chip sees and indicates a connectivity problem.

A more familiar way to visualize the result is by using a color-coded map (**Figure 8**). Red represents unacceptably high $R_{EFF}$; blue represents results within specification and with acceptable $R_{EFF}$. This **figure** depicts the $R_{EFF}$ for a small block of a design. Black areas contain no instances. Blue areas signify four evenly spaced vertical power trunks. Between the vertical trunks, the resistance rises slightly, as you would expect, resulting in the three vertical green areas.

However, at the lower left, an orange-and-red area indicates high resistance, which occurs in one pair of rows. In all other rows, the left edge connects directly to the vertical power bus, but in these rows, it does not. Missing vias, where the left and left-center trunks *should* have vias connecting them to the horizontal power lines, cause the problem.

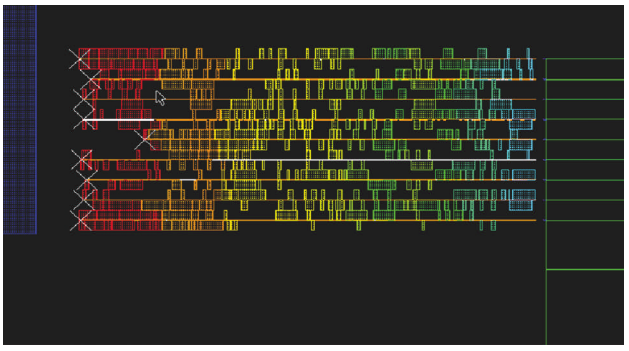

Figure 10 The $R_{EFF}$ map and trace-back indicate that only the power trunk on the right side supplies this group, causing it to see high $R_{EFF}$.

Another method of making the results useful is to perform differential $R_{EFF}$ analysis ($dR_{EFF}/dx$) by analyzing the raw $R_{EFF}$ results. This approach finds cases in which the actual $R_{EFF}$ values of two neighboring pins are not high, so they would neither show up as red in the $R_{EFF}$ map nor show up outside the main region in the $R_{EFF}$ histogram. However, their difference is higher than you would expect, meaning that current is taking different paths to these pins even though the pins are

very close to each other. This situation indicates a potential network defect.

## RESISTANCE TRACE-BACK

In formal verification, trace-back should accompany any violation of an assertion in which the tool generates information the designer can use to inspect the problem. **Figure 9** shows an example of a trace-back overlaid on an $R_{EFF}$ map for debugging.

In the **figure**, the three instances at the upper right appear marked and in red. The **figure** shows traced and highlighted $R_{EFF}$ paths. This trace-back shows that a power trunk at only the left side drives the power rail the instances connect to, and current travels to these instances by following a more resistive path than that of the other instances. The instances can't reach the power trunk at the right because a macro blocks it.

The two other markers at the rail below represent instances with lower $R_{EFF}$. The **figure** highlights their trace-backs, as well as points of comparison with the higher $R_{EFF}$ instances. In **Figure 10**, the $R_{EFF}$ map and trace-back indicate that only the power trunk on the right side supplies this group, causing them to see high $R_{EFF}$.

There is no question that power-grid verification is getting harder. New formal power-grid techniques will be powerful additions to engineers' toolboxes, providing the ability to prove assertions about the entire power grid and pinpoint problems early in the design flow with fast turnaround times and vector independence.

Formal grid verification provides an early checkpoint in the design flow at which a user can sign off on the structural integrity of the power grid before proceeding to voltage-drop and electromigration analysis. Formal grid verification would discover these problems, and that fact directly affects these analysis results, eliminating unnecessary voltage-drop- and electromigration-simulation iterations later. You'd eventually find the problem but only after long simulation runs, tedious debugging, and postprocessing.EDN

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## AUTHOR'S BIOGRAPHY

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# Quiet-node current sensing tames noise problems

WHERE YOU LOCATE THE CURRENT-SENSE RESISTOR IN YOUR DC/DC CONVERTER CAN HAVE A PROFOUND EFFECT ON THE DEVICE'S PERFORMANCE.

In designing dc/dc converters, one of your options is the CMC (current-mode-control) method. PCMC (peak CMC) offers some well-known benefits as well as drawbacks. When compared with VMC (voltage-mode control), CMC more quickly satisfies demands to supply load-current transients. With CCM (continuous-conduction-mode) operation, the VMC error amplifier generally requires a Type 3 compensation network, which comprises three poles and two zeros. A ceramic output-filter capacitor requires only two poles and two zeros. You can implement this transfer function with a resistor and two capacitors around the error amp, and a parallel RC (resistor/capacitor) between the LC (inductance-capacitance) output and the error-amp input. With a PCMC converter operating in CCM with a ceramic output capacitor, the capacitor across the resistor from the LC output to the error-amp input is unnecessary. PCMC requires two poles and only one zero for compensation. Thus, the PCMC error-amp-compensation network is generally simpler than its VMC counterpart. PCMC is more complex because you must compensate the slope of the inner loop.

Because the PCMC error amp recovers more quickly than does that of the VMC, PCMC reduces compensating-capacitor overcharging when the error amp saturates during large load-current transients. Also, compared with VMC—except for input-fed-forward VMC—PCMC corrects sooner for input-voltage changes and disturbances. With symmetrical transformer-coupled converters, such as full-bridge, half-bridge, push-pull center-tapped, and associated variations, PCMC corrects volt-second asymmetry in the PWM (pulse-width-modulated) drive, preventing magnetic-core saturation known as stair casing or flux walking.

With PCMC, clamping the error amplifier's output easily provides inherent pulse-by-pulse current limiting. Also, in CCM, PCMC eliminates the complex-conjugate, high-Q, low-frequency double pole that the VMC's LC power stage forms, leaving a single low-frequency RC pole and a complex-conjugate double pole at or near the Nyquist frequency (half the switching frequency). The result in general is improved dynamics. Also, using PCMC or ACMC (average CMC) allows paralleling several power stages to obtain increased output current.

As desirable as these benefits are, PCMC exhibits some limitations that you shouldn't ignore: The state variable that you should control is the average—not the peak—inductor current. However, with proper design techniques, as long as you maintain CCM, controlling the peak value can be as effective as controlling the average. Should the load current decrease to the point of DCM (discontinuous-conduction mode), the voltage-control (outer) loop, which is generally slower than the current-control (inner) loop, must correct an associated peak-to-average error, partially negating PCMC's speed benefit. Also, you must employ slope compensation to optimize load-current and input-voltage dynamics, as well as to ensure the current-control loop's unconditional stability. To optimize load-current and input-voltage dynamic response, the compensating ramp's slope should be 50% of the inductor current's equivalent downward slope. However, to maintain stability and sufficient damping in the current-control loop, a ramp-slope value of 50% works effectively only for duty factors less than approximately 36%. Above 36%, the required ramp slope must exceed 50%, which compromises the load current's and input voltage's dynamic response.

You encounter another PCMC shortcoming when the input voltage varies over a wide range. To ensure CCM operation at high-line input, deep-CCM operation occurs at low-line input. The ramp of the sensed-current signal becomes shallow, and SNR (signal-to-noise ratio) suffers. Using a current-sensing resistor with a larger value improves SNR at the expense of increased dissipation and lower efficiency. Also, with half-bridge converters that use a floating or soft (capacitive) center point, PCMC can cause the capacitive midpoint voltage to "walk" into either rail.

## PROPER DESIGN OVERCOMES LIMITATIONS

PCMC's limitations are substantial, but proper design tech-

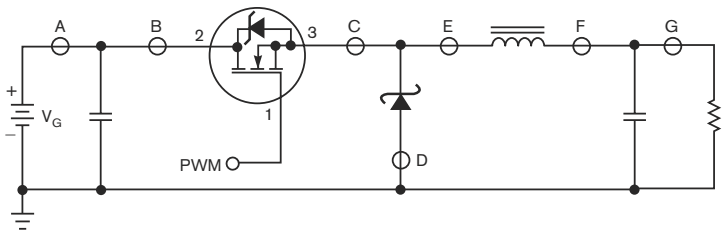


Figure 1 In a buck converter, you can obtain the inductor-current waveform by sensing the power-switch current, which equals the inductor current during the power switch's on-time.

niques can overcome all of them. However, one remaining problem has plagued PCMC since its invention and has caused some designers to abandon the approach altogether and instead employ VMC or ACMC. This problem is the leading-edge spike on the sensed-current waveform as the power switch turns on. This spike is large enough to prematurely terminate the PWM pulse before regulation. Because of output droop, the error signal on the next pulse is larger, and the pulse is longer. Over many cycles, the result is PWM-pulse jitter, which is quite visible on a scope.

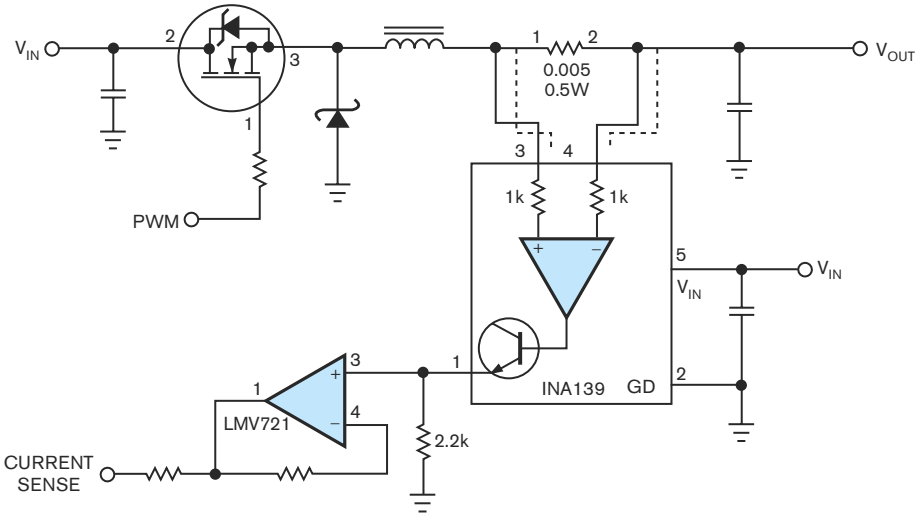


Figure 2 By using a low-valued sense resistor and locating an instrumentation amplifier very near the resistor, you can sense the dc/dc converter's output current with low noise and low power dissipation.

One way of dealing with this spike is to use leading-edge blanking, which momentarily disables current sensing at the leading edge of power-switch turn-on, preventing premature turn-off. One problem with this approach is that it imposes a minimum duty-cycle limit. Because the current-sense function is effectively blind at the moment of power-switch turn-on, a minimum pulse-width value exists. This problem, which exists at very light loads or no load, causes the output capacitor to overcharge, because the duty cycle cannot be low enough. Also, the occurrence of a fault, such as a direct short circuit on the output, delays current limiting, resulting in possibly destructive power dissipation. In many cases, this trade-off is sometimes undesirable. If a converter must operate without a minimum-duty-cycle limit, needs fast-acting fault protection, or both, then leading-edge blanking is undesirable.

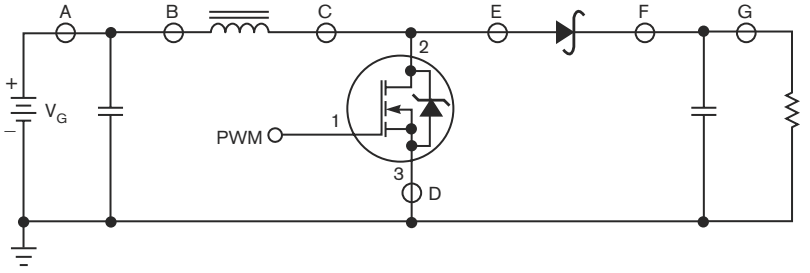


Figure 3 In a boost converter, locating the sense resistor in the conventional place yields suboptimal performance. The best location is Point B.

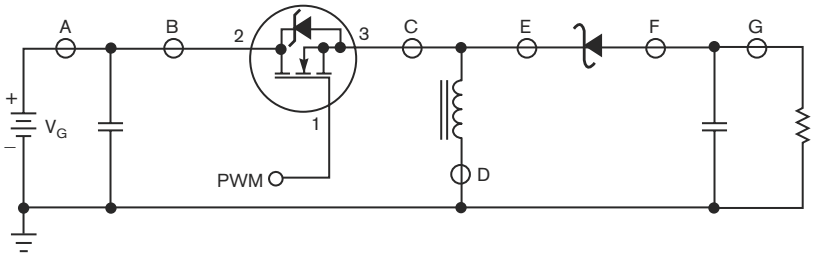


Figure 4 With the inverting buck-boost topology, the sensing locations have traditionally been B for PCMC and D for ACMC. Using D for PCMC produces quiet-node benefits, albeit with increased dissipation.

Another commonly employed method is RC filtering of the spike. The problems with this approach are similar to those of leading-edge blanking. If the RC time constant is long enough to adequately suppress the spike, it is generally long enough to delay turn-off in response to an output short circuit. Also, as with leading-edge blanking, a long time constant can impose a minimum duty-cycle limit, which is undesirable at light loads. One additional problem is that the RC time constant adds a pole to the current-loop transfer function. This pole with its associated phase lag can produce instability or underdamped response. To ensure stability, the time constant should be short, so that the associated pole resides at a high frequency, well above the unity-gain bandwidth. In that case, the problem is that the short time constant provides only a limited amount of filtering of the

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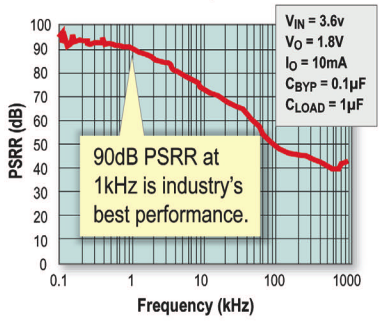


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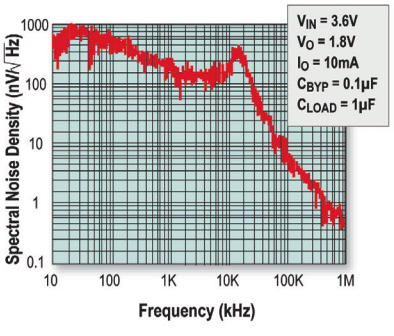


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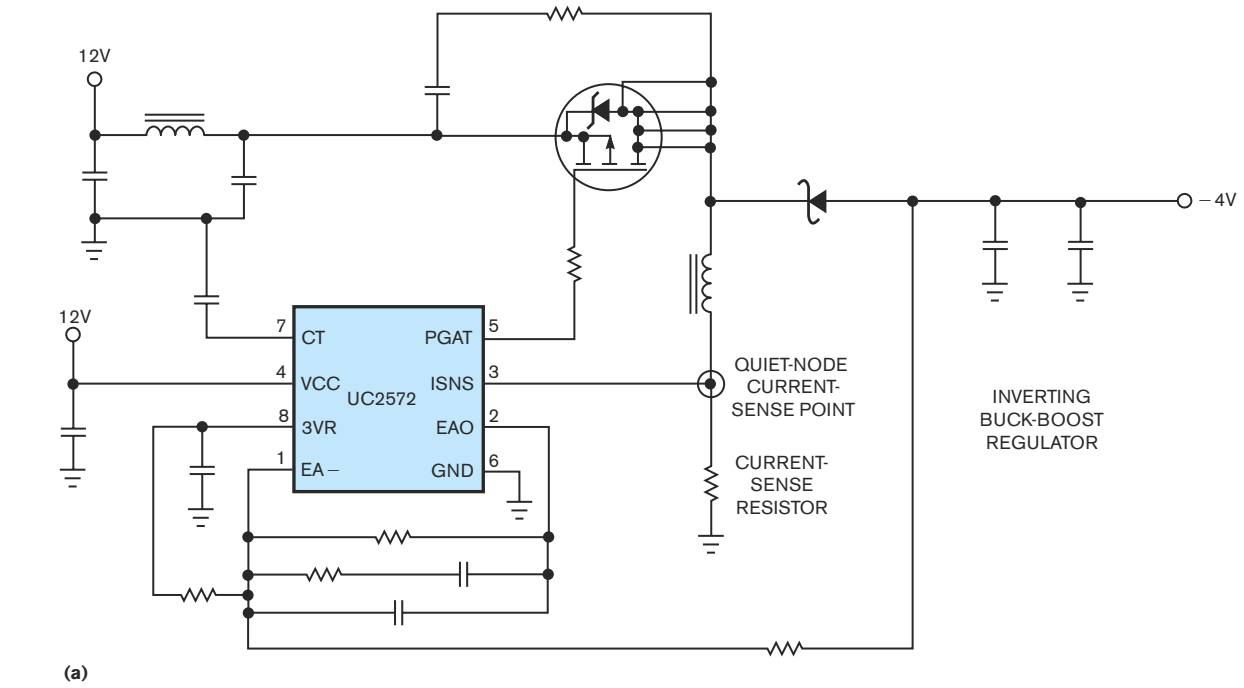
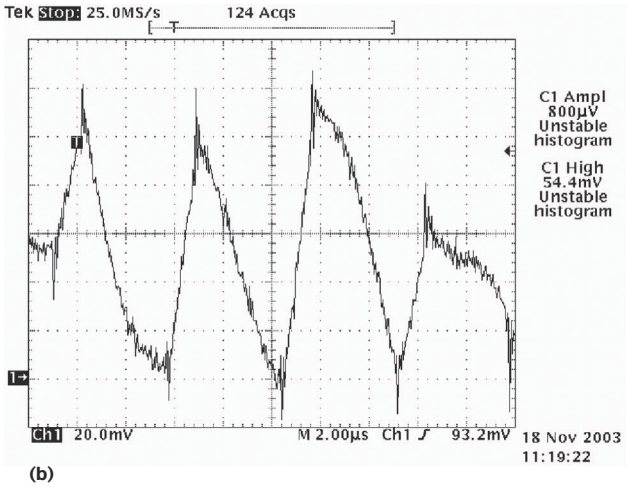
spike. You must usually seek another approach to the leading-edge current-spike problem. Some engineers correctly call this issue the bane of PCMC. Without a doubt, it is the most severe limitation they will encounter with PCMC. It is a result of the current-sense element's location; relocating that element provides the solution.

## FINDING THE BEST SENSE-RESISTOR LOCATION

Begin with the buck topology, which allows locating the current-sense resistor in several places. For PCMC, the most popular location is Point B (**Figure 1**). You obtain the inductor-current waveform by sensing the power-switch current, which equals the inductor current during the power-switch on-time. This location results in low power dissipation, because current flows in the sense resistor only during the on-time, and no current flows during the off-time. With low-duty-cycle converters, this location is advantageous. Also, because of the pulsating current, you can use a current transformer, allowing a sense-resistor value that further reduces dissipation. Finally, the common-mode voltage at B is stable, equal




(a)

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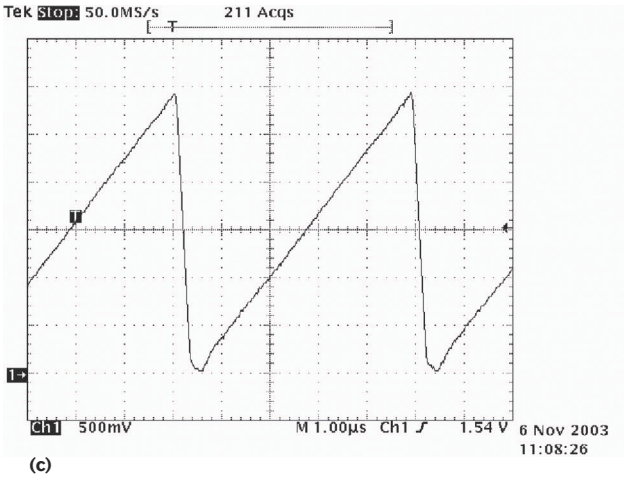


(c)

Figure 5 In this inverting buck-boost voltage-mode converter, a common sense-resistor location is in series with the output inductor (a). The sensed-current wavefore (b) is not beautiful but has no nasty current spike. The jagged edges are measuring artifacts. A second oscillogram (c) depicts the sawtooth-oscillator voltage waveform.

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to the value of the input-voltage source during both the on- and the off-times. For PCMC, engineers have extensively used B and consider it optimum.

Now, examine Point F (**Figure 1**) for current sensing: Engineers traditionally use this location for ACMC. The advantages are that F has a stable common-mode voltage, roughly equal to the output voltage during both the on- and the off-times. Also, F represents the average inductor current, which equals the average output-load current. Additionally, the entire inductor-current waveform is sensed, which is necessary for ACMC but not for PCMC. For ACMC, F, a quiet node, is the optimum location.

Now, examine the disadvantages of B and F. With B, the sensed current is pulsed. The current in the sense resistor increases abruptly when you turn on the power and decreases abruptly when you turn it off. Power-switch inductance and neighboring stray inductance combine with this switching action to produce a large turn-on spike on the leading edge. Attempts to filter this noise spike produce only limited success. With current sensing at F, the power dissipation is larger than at B, because conduction and dissipation occur for the entire cycle, versus only during the on-time. Also, at F, a nonzero dc average value exists, and no switching takes place, precluding the use of a current transformer. For these reasons, B is popular for PCMC, and F is popular for ACMC.

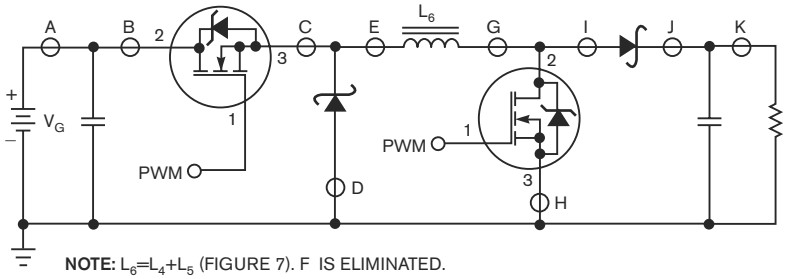


Figure 6 In the noninverting buck-boost topology, it at first appears that there is no acceptable sense-resistor location.

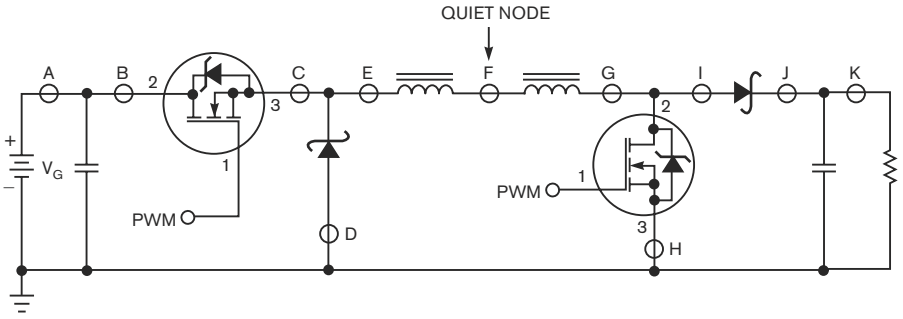


Figure 7 If you can replace the output inductor with two inductors, each having half the value, placing the sense resistor between them yields optimal results.

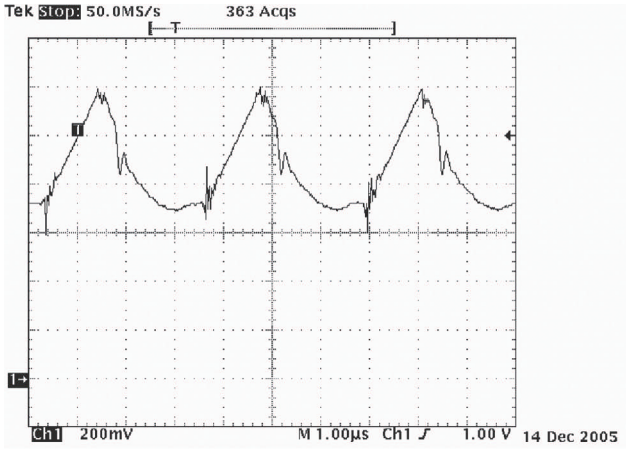


Figure 8 This current waveform shows that the instrumentation amplifier nicely rejects the small common-mode variation that appears at both ends of the sense resistor.

One salient advantage with F is that there is no turn-on spike. Because the sense resistor in F is directly in series with the inductor, neither a turn-on spike nor a turn-off spike occurs. One way of eliminating the spike with PCMC is to use F for current sensing, as ACMC does. The price is higher dissipation, but recently introduced instrumentation amplifiers have alleviated this problem. By using a low-valued sense resistor and locating the instrumentation amp near the resistor, you can obtain low noise and low dissipation (**Figure 2**). One suitable such amplifier is Texas Instruments' (www.ti.com) INA139. The differential, transconductance amp has an input-common-mode range that exceeds the supply. The transconductance value, $g_M$, is 1 reciprocal kΩ, or 1 mS (millisiemen). The specified gain-bandwidth product is 4.4 MHz. Should this value be insufficient for your application, you can use an additional single-ended op amp in addition to the instrumentation amp. This quiet-node sensing technique produces a waveform relatively free of switching noise.

The price you pay, in addition to the expense of the amplifier, is sense-resistor current, which flows throughout the cycle, increasing the dissipation and, in some cases, the cost of the additional op amp you need to provide additional gain.

## BEST FOR AVERAGE AND PEAK CONTROL

Now, focus on the boost-converter topology (**Figure 3**). The quiet nodes for this topology are A and B. For sensing

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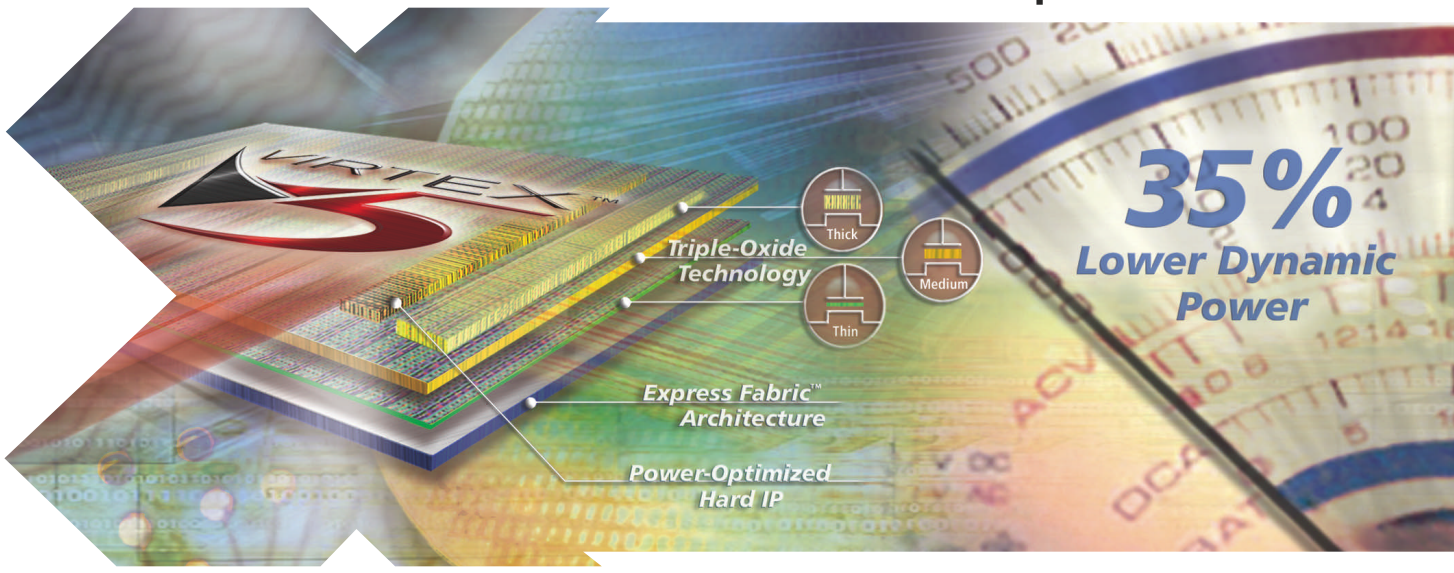


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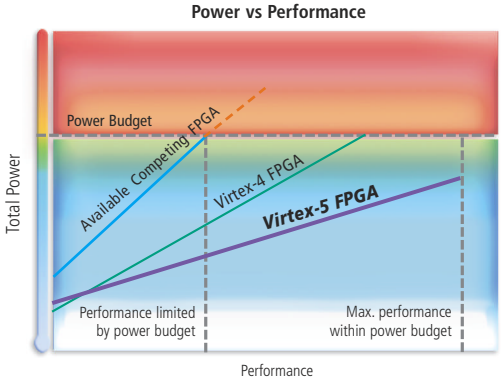


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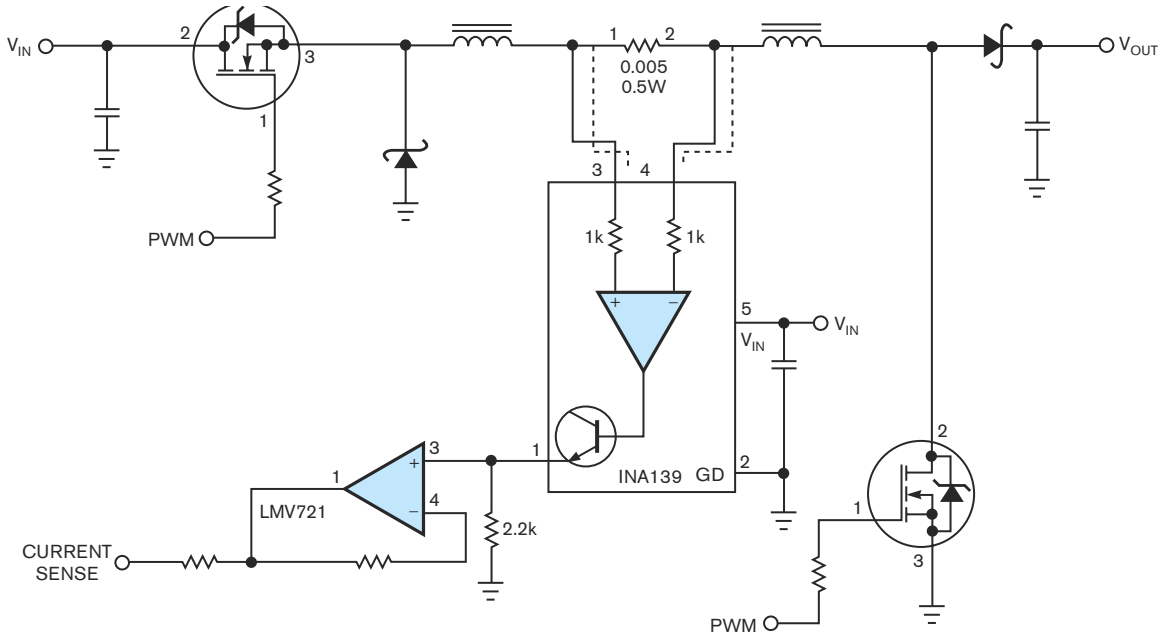


Figure 9 In this noninverting buck-boost converter, the optimal location for the sense resistor and booster-amplifier input is between the two series output inductors.

inductor current, B is optimum and is the choice location for ACMC. PCMC traditionally employs D, but you should use B for PCMC, as well. Note that B is in series with the inductor and has a fixed common-mode voltage, so that the current waveform does not contain the leading-edge spike. Again, power dissipation at B is greater than at D because of conduction over the entire cycle.

With the inverting buck-boost topology (**Figure 4**), the sensing locations have traditionally been B for PCMC and D for ACMC. Using D for PCMC gives the quiet-node benefits, albeit with increased dissipation. One commercially available PWM-control IC dedicated to inverting buck-boost operation—Texas Instruments' UC2572 series—uses this location for current sensing (**Figure 5a**). It is a VMC type with direct duty-cycle control rather than input feedforward control. The current-sense waveform appears in **Figure 5b**. Once again, the normal location for ACMC is actually optimum for PCMC, as well (**Figure 5c**).

Now, turn your attention to the noninverting buck-boost topology (**Figure 6**). As far as sensing inductor current goes, the location possibilities include B, C, D, E, G, H, I, and J. Unfortunately, all of these locations carry a disturbance, either current- or voltage-related. Locations B, D, H, and J have a quiet voltage but pulsating current, which is prone to the turn-on spike. Nodes C and I have the same noisy current, plus a pulsating voltage, switching from $V_G$ to ground. Nodes E and G have quiet currents but pulsating voltages. Unfortunately, none of the locations offers both quiet current and quiet voltage. There appears to be no good location for current sensing.

However, if you recall how you derive a noninverting buck-boost inverter, you observe the following: The converter is merely a cascade of a buck stage followed by a boost stage (**Figure 7**). With the buck stage, an inductor is in the output, whereas, in the boost stage, an inductor is in the input. If you observe the midpoint of the two series inductors, you see that Node F, the midpoint of the two series inductors, has a quiet current because it is between two inductors. Also, the voltage is quiet and stable. During the switch's on-time, Node E is near $V_G$, and Node G is near ground, so the voltage at Node F is about half of $V_G$. During the switch's off-time, Node E is near ground, and Node G is near the output voltage, $V_O$, so that F is about half of $V_O$. If the input voltage, $V_G$, spans 9 to 16V, then during the on-time, Node F is at about 4.5 to 8V. If the output, $V_O$, is 12V, then, during the off-time, Node F is at about 6V. The voltage at F is not absolutely constant but certainly is steadier than the voltage anywhere else. As the current waveform of **Figure 8** shows, the instrumentation amplifier rejects the small common-mode variation. Hence, for the noninverting buck-boost converter, the optimum location, or quiet node for current sensing, is the midpoint of the two series-connected inductors. Unfortunately, combining the two inductors into one inductor with twice the value often eliminates this quiet node, an undesirable consequence. Instead, if you realize the inductive energy-storage element as a pair of series-connected inductors, their midpoint offers a quiet node for optimum current sensing. Place the sense resistor and instrumentation amplifier as **Figure 9** shows.

**Figure 8** depicts a prototype for the noninverting-buck-boost-converter topology with quiet-node current sensing, and **Figure 9** shows the corresponding current-sense waveform. On a scope, the waveform is quiet, stable, and free of jitter. It looks much like a VMC sawtooth waveform (**Figure 5c**), which is quiet and jitter-free. The switching-node pulse waveforms are also stable, with low jitter. The converter in this example accepts inputs of 9 to 16V and produces 12.1V at 4A. At low-line input, the duty factor is 0.6, or 60%, and the power loss in the current-sense resistor is 0.303W. If you place the resistor at B, the traditional PCMC practice, power loss would be 0.182W, a difference of 0.121W. With the output power of 48.4W, 0.121W constitutes an efficiency penalty of just 0.25%. At high-line input, the power loss is 0.166W with a 0.452 duty factor. Sensing at B gives a loss of 0.075W, a 0.091W differential. The efficiency penalty is a mere 0.19%.

**The leading-edge noise spike, the most severe problem you encounter with PCMC, is a direct result of the location of the current-sense resistor.**

For nonisolated dc/dc converters using PCMC, the leading-edge noise spike, the most severe problem you encounter with PCMC, is a direct result of the location of the current-sense resistor. Relocating this resistor to a point you traditionally use for ACMC eliminates the leading-edge spike and greatly improves SNR performance at the cost of increased dissipation. Using an instrumentation amplifier close to a low-valued resistor minimizes this penalty. A noninverting buck-boost topology traditionally implements the power-stage inductor as a single component. Using a series-connected pair of inductors, each half the value of the single part, eliminates the leading-edge turn-on-current spike and realizes a quiet node at the inductors' midpoint, making it possible to obtain PCMC with low noise. Until now, this goal had been unattainable. EDN

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## AUTHOR'S BIOGRAPHY

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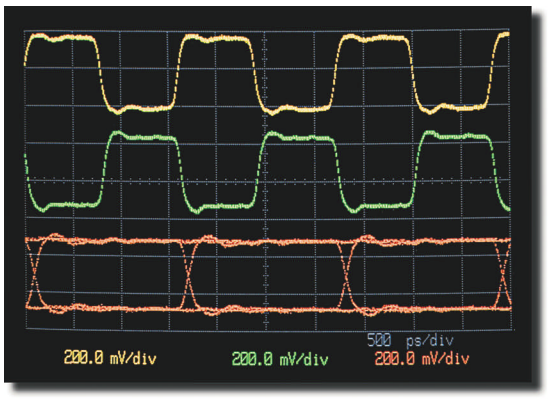
- ***80 ps rise and fall times***
- ***16-digit frequency resolution***
- ***CMOS, LVDS, ECL, PECL, RS-485***
- ***Phase adjustment & time modulation***




*Plot shows complementary clocks and PRBS (opt. 01) outputs at 622.08 Mb/s with LVDS levels. Traces have transition times of 80 ps and jitter less than 1 ps (rms).*

The CG635 generates clock signals—flawlessly. The clock signals are fast, clean and accurate, and can be set to standard logic levels.

***How fast?*** Frequency to 2.05 GHz with rise and fall times as short as 80 ps.

***How clean?*** Jitter is less than 1 ps and phase noise is better than –90 dBc/Hz (100 Hz offset) at 622.08 MHz.

***How accurate?*** Using the optional rubidium timebase, aging is better than 0.0005 ppm/year, and temperature stability is better than 0.0001 ppm.

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BY BOGDAN GAVRIL • ELMA BUSTRONIC

# Maintaining channel compliance in high-speed backplanes

THE ADVENT OF SWITCHED-FABRIC OPTIONS HAS GEOMETRICALLY INCREASED DATA RATES. AS SPEEDS INCREASE ACROSS THE BACKPLANE, IT BECOMES MORE CHALLENGING TO MAINTAIN HIGH SIGNAL QUALITY. THEREFORE, THE ROLE OF DESIGN ENGINEERING FOR BACKPLANES IS EVOLVING.

Applications such as data acquisition and processing, communications, and video streams are driving intense bandwidth demands. Regardless of the physical limits, system manufacturers must provide the means of accommodating these data rates, whereas the backbone, including the backplane and the enclosure, has commonly stayed with the same form factor and available space. Legacy-bus architectures, such as VME and CompactPCI, cannot handle the data rates of today's high-speed silicon. (However, new architectures, such as VXS for VME and CompactPCI Express for CompactPCI, use new, high-speed connectors to add data planes to these backplanes, which preserves the legacy bus and provides high performance.) Since 1981 with VME and 1998 with CompactPCI, a backplane designer had to follow design rules, understand the specification and components, maintain proper impedance levels, and sometimes use creative design to resolve space constraints. But today's designs require much more to ensure adequate performance.

The whole engineering process for backplane design must adapt to the challenges that the new high-speed technologies bring. The specification for a backplane design may indicate the amount of data specified drivers carry at a given speed, under its particular form factor. But there are many more considerations, including some sort of assurance that the backplane will perform properly. You also need to know whether it will work well with the other cards in the system.

With backplane speeds hitting 10 Gbytes/sec and beyond, maintaining channel compliance is a challenge. When carrying 10 Gbytes/sec per one differential pair, the length is a benchmark from which to start. In fact, every discontinuity in the backplane is a measuring stick. The longer the path, the bigger the influence of the surrounding environment of the signal. The length of the signal path brings greater risk of crosstalk along the signal and attenuation due to connector and dielectric losses. It can also affect the reference planes and the return path. The high signal density and topologies of today's high-performance designs often require more layers for the routing, leading to thicker backplanes. This situation, in turn, exacerbates the stub effect, which becomes problematic for maintaining signal integrity at speeds exceeding 5 Gbytes/sec. There are ways to improve the signal performance other than adding layers and making the backplanes thicker. Examples include the use of high-grade materials, design practice to reduce the stub effect, and counter drilling.

With thicker backplanes, the length of via stubs is greater (**Figure 1**). You can minimize the resulting stub effect by choosing a laminate with a lower dielectric constant which allows you to achieve the 100Ω differential impedance with thinner pc-board layers. A lower dielectric constant is not the only characteristic that makes higher performance board materials attractive. High-grade materials, such as Nelco (www.nelco-usa.com) 4000-13SI, Rogers (www.rogerscorporation.com) 4350, and others, have significantly lower loss tangent values at these higher frequencies. The loss tangent value indicates a degree of undesirable interaction with

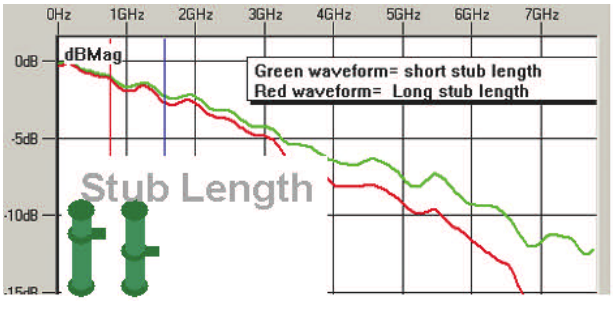


Figure 1 Thicker backplanes use longer via stubs.

a signal at a given frequency. The manufacturers of the first prototypes of the VXS backplane used Nelco 4000-13SI to maximize performance (**Figure 2**). They developed other versions in standard FR4, and these versions still maintain excellent signal integrity.

## SIMULATION AND PRELAYOUT ANALYSIS

When working with new high-speed technologies, the backplane designer needs to complete some upfront work before he begins routing the lines of the backplane. A signal-integrity engineer needs to provide impedance calculations and define the proper geometries and layer structure. By simulating the foreseen data patterns under the speed and signal requirements, the signal-integrity engineer can recommend the ideal topology and adjust the initial estimation. This process includes taking into account the length of the traces, the risk of crosstalk, and the ground references. The engineer then recommends the best path to minimizing the stub effect or any potential problem areas.

A key factor in defining the impedance and the geometries is the material that you use. The characteristics of the material and the tolerances of the fabrication process are important. Therefore, you should maintain close contact with the fab shops throughout the design.

## SIMULATION AND POSTLAYOUT ANALYSIS

When the layout is complete, the signal-integrity engineer can simulate the whole fabric. He will create the models for the vias, the through-holes, and the fabric, and, using the existing models of the connectors and transceivers, he will run the simulations for various parameters, such as jitter, ringing, overshoot, eye diagrams, and S parameters, for the whole signal pattern. If the original design rules are implemented correctly, the simulation results will look as expected. Signal-integrity analysis can provide the customer with a proof of the backplane's ability to properly function before fabrication.

After analyzing the requirements, the design engineer recommends a basic architecture and the necessary number of links over connectors that fit the form factor. He has to choose the type of fabric, the connectors, and the pc-board material. The design engineer must also be involved in parts sourcing. He needs to choose not only components with the right performance specifications, but also components that fit within the cost structure and manufacturability of the design. Further, he must view a backplane in relation to its environment. All the parts need to work together. Important considerations include shelf managers or system monitors, the dimensions in relation to the chassis, hot swappability, and thermal management.

## BACKPLANE CHARACTERIZATION

Once you fabricate the backplane and assemble the connectors and components, it's time to measure the performance of the backplane. Even if the postlayout simulations show strong results, it is mandatory to validate the design through measurements. Doing so provides not only proof that assumptions and design techniques are correct, but also a

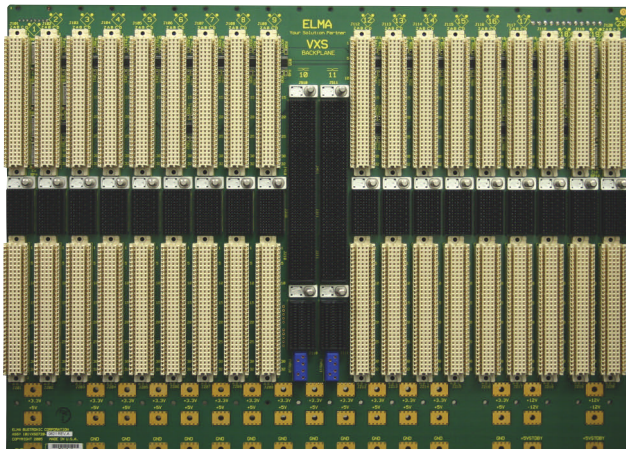


Figure 2 Using a high-grade material, such as the one in this backplane, can provide lower loss-tangent values at high frequencies, translating into cleaner signals.

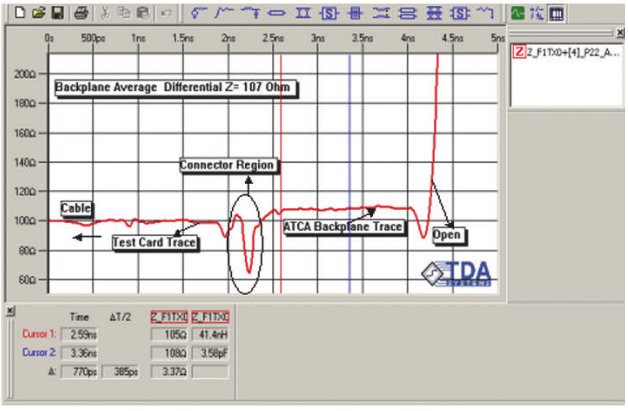


Figure 3 The correlation between simulation and measurement is excellent with equivalent circuit models of a lossy backplane.

verification of the fabrication process. You assume that a fab shop will follow the constraints, but the material and fabrication tolerances may affect the signal integrity. Matching the simulations with the measurements is one of the goals of the design process. Finally, it provides proof for the customer of the high performance of the backplane.

Consider the backplane-design example in **Figure 2**, a five-slot replicated Mesh ATCA (Advanced Telecom Computing Architecture) backplane. The first measurement to consider on the five-slot ATCA backplane is the fabric impedance. The ratio of the voltage and current at any point as a test pulse travels down a pair of differential-backplane traces defines the characteristic impedance of the transmission line. Impedance mismatches due to vias and connectors and variations can cause reflections, which degrade the signal quality.

TDR (time-domain reflectometry) produces a positive incident wave that you apply to the DUT (device under test). The step pulse travels down the DUT at the velocity of prop-

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agation of the line. At every impedance discontinuity that the signal encounters, part of the incident wave reflects. The reflected voltage wave appears on the oscilloscope. The resulting waveform is like a road map of the impedance variations across the trace. If the load impedance is equal to the characteristic impedance of the line, no wave reflects. All that appears on the oscilloscope is the incident voltage step the scope records as the wave passes the monitoring point.

To get the worst-case scenario, you test the longest net traces. The measurements use a wide-bandwidth oscilloscope with 18-GHz measuring bandwidth, high-quality cables, termination resistors, and IConnect analysis software from TDA Systems, a part of Tektronix (www.tek.com). Per the ATCA specification, the differential impedance of the backplane and board serial links for base and fabric interfaces should be 100Ω±10%. The measured average value of differential trace line comes out to 107Ω. Therefore, even the worst-case scenario is within the required range (**Figure 3**).

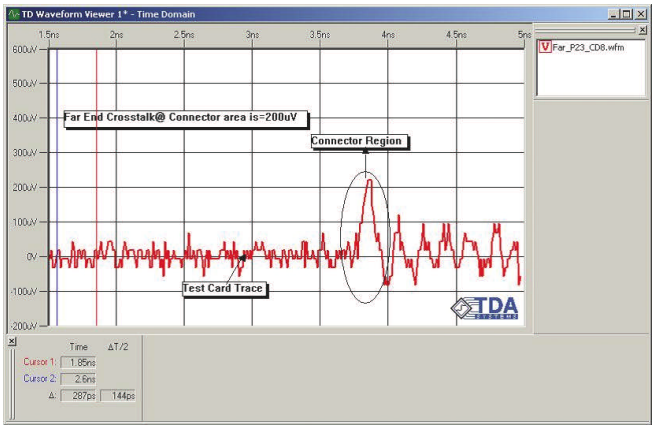



Figure 4 The result of the far-end crosstalk of a five-slot ATCA backplane shows that neither the insertion nor the return loss violates the insertion loss and return limits for PICMG 3.0.

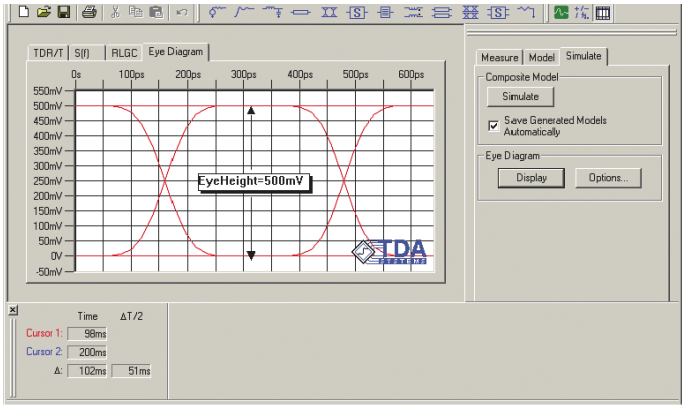
## CHARACTERIZATION–CLOCK IMPEDANCE

The ATCA architecture includes six synchronization-clock buses that divide into three groups of two differential pairs each. You implement each clock bus as a differential pair that connects to all slots through pins in the Zone 2 connectors. The buses are fully symmetric so that receivers and transmitters (bus drivers) can reside in any slot. The first pair of clock buses, Clock 1A and Clock 1B, is dedicated to redundant 8-kHz system-clock signals. This frequency is the fundamental frequency that all digital-telephony-transmission systems use. The differential impedance of the backplane serial links for the clock interfaces on the backplane should be 130Ω±10%. The measured average value of clock-trace line in the five-slot example is 124Ω. Again, the results are well within the limits.

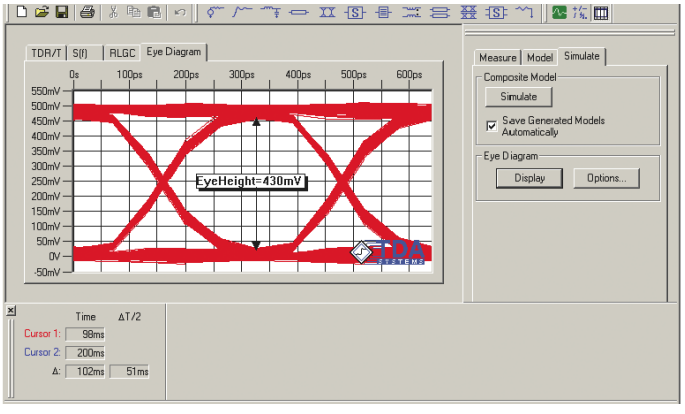
Scattering parameters can capture the reflection and transmission from junctions in backplanes. The ratio of the reflected power to the incident power is the return loss, and the ratio of the transmitted power to the incident power is the insertion loss. You derive these values for defined incremental frequency steps over a range of frequencies that covers the design requirements for the backplane. For ATCA, this range is 0 to 5 GHz.

"Crosstalk" refers to undesired signals induced on traces or paths due to other nearby signals. "Near-end (backward/reversed) crosstalk" refers to the crosstalk on the victim line at the end closest to the driver, or the aggressor line. "Far-end (forward) crosstalk" refers to the crosstalk on the victim line farthest away from the aggressor. To achieve accurate results, use high-quality cables, termination resistors, and adapters with the pc board under test. **Figure 4** shows the result for far-end crosstalk. The characterization results also show that neither the insertion nor the return loss on the five-slot ATCA backplane under test violates the insertion loss and return limits for PICMG (PCI Industrial Computer Manufacturing Group) 3.0.

From the far-end-crosstalk graph, the aggressor amplitude



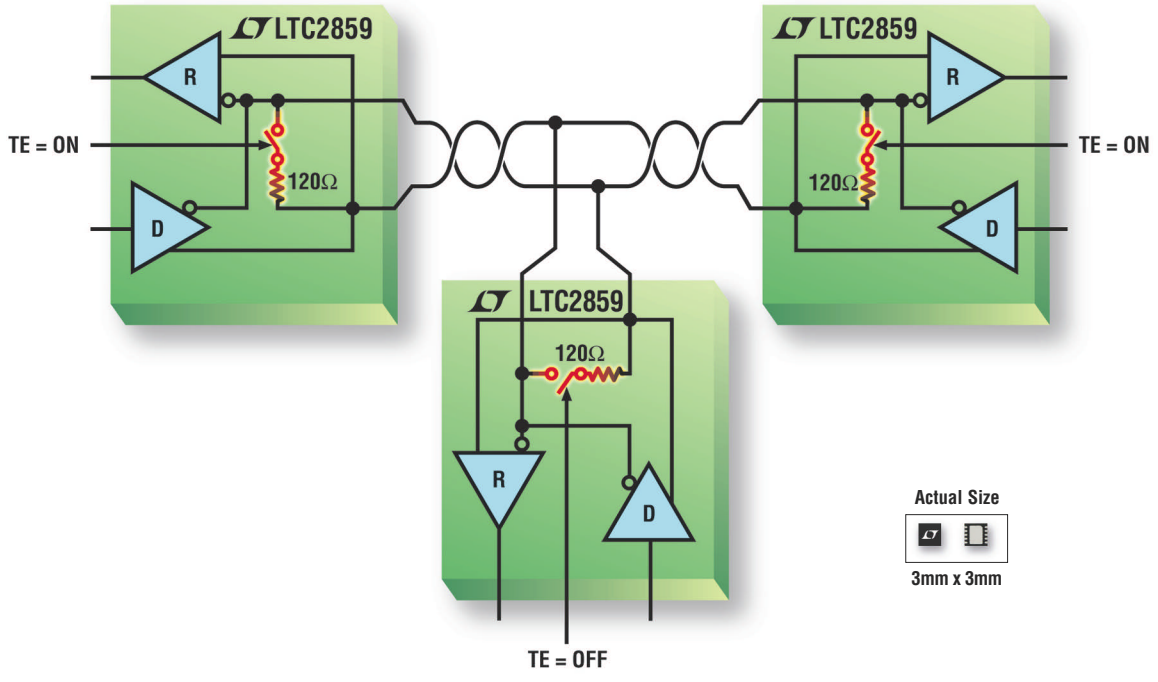

(a)




(b)

Figure 5 The various trace lengths have eye heights of 500 mV (a) and 430 mV (b). The larger the eye opening, the better the results. Even the worst-case trace has excellent results, well within specifications.

# RS485 with Switchable Termination

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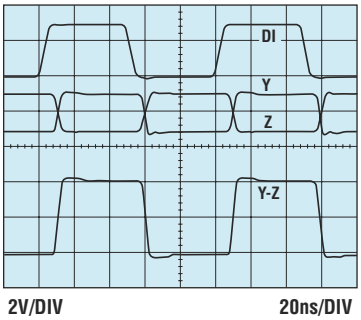


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is 200 mV, and the crosstalk in connector area and backplane-trace area are negligible—that is, only microvolts. From your next measurement, the aggressor amplitude is 200 mV, and the crosstalk in the connector area is 4 mV, or only 2%.

## EYE DIAGRAM

An eye diagram superimposes each bit period in the results of a simulation, which a long, multicycle bit sequence drives, over the top of all others—like a timed-exposure photograph—and presents waveforms that have open areas shaped something like a human eye. The larger the eye opening, the better the results. The most common type of stimulus that eye-diagram generation uses is the PRBS (pseudorandom bit sequence). The results show that the trace on layer nine, which routes on slots 1 to 5, still has a more than adequate eye opening at 86% at a PRBS of $2\times10^{-1}$, or 3.125 Gbps.

As you can see from **Figure 5**, the five-slot ATCA-backplane performance is well within the specified requirements, even taking into consideration the worst-case scenarios. Simulation and characterization will be increasingly important as the industry continues to move to higher speed switch-fabric technologies.

For design engineers, just using routing skills is not enough anymore. A modern design engineer must have expert knowledge of signal integrity, signal propagation, power distribution, architectures, connectors and components, materials properties, and fabrication processes. Each engineer has to thoroughly know all the applicable standard specifications and must be able not only to follow the signal-integrity recommendations, but also to work to define the necessary geometries and layout guidelines. The design engineer often has to interact with the customers, so a deep understanding of the whole picture is valuable.

Each design is part of the learning process. With each application, the engineers learn and gain experience.

A MODERN DESIGN ENGINEER MUST HAVE EXPERT KNOWLEDGE OF SIGNAL INTEGRITY, SIGNAL PROPAGATION, POWER DISTRIBUTION, ARCHITECTURES, CONNECTORS AND COMPONENTS, MATERIALS PROPERTIES, AND FABRICATION PROCESSES.

Measurements can be proof of accurate simulation techniques, or they can show that adjustments are necessary. By comparing the postlayout simulations with the measurements, you can provide valuable feedback to fab shops, improving the response and precision and allowing a better estimation of the fabrication impact on the final product. The customer will receive a product with superior performance in less time and with the guarantee to meet or exceed the specifications. EDN

## AUTHOR'S BIOGRAPHY

*Bogdan Gavril is the director of engineering for Elma Bustronic (Fremont, CA) and has been with the company since October 2004. He leads the engineering team in implementing new technologies, continuously improving design quality and techniques, and expanding the company's signal-integrity initiative. Although Gavril is new to Elma Bustronic, he has been with parent company Elma for more than four years. He started at renowned European backplane company TreNew in 1997 as a designer before Elma acquired the company in 2000. Gavril served as managing director of the Romanian Design Center, now Elma Romania, and received his degree in electronics technologies from the Polytechnic University of Bucharest (Romania).*

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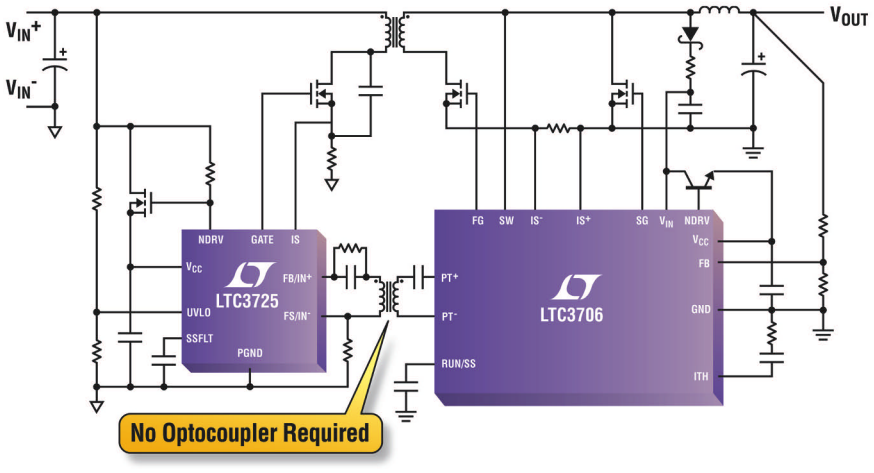


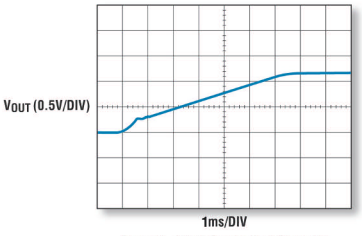


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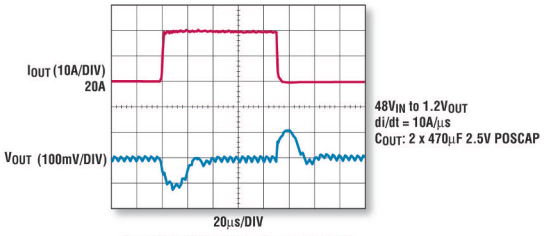


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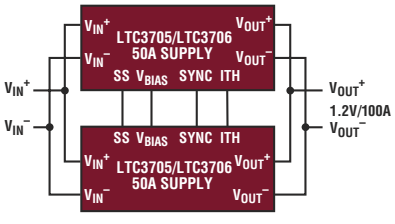


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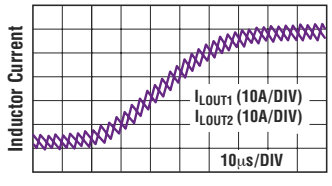


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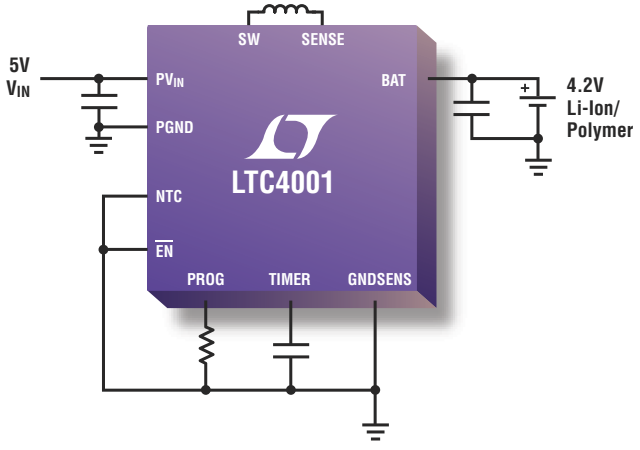


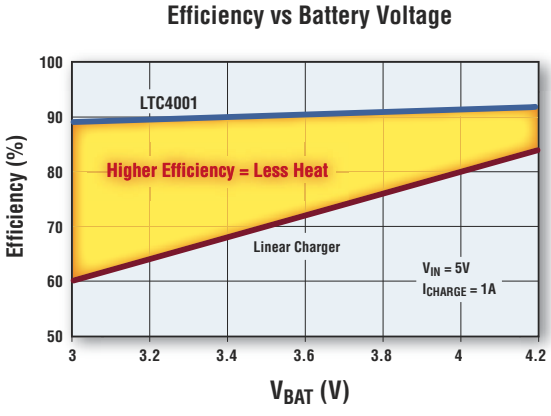


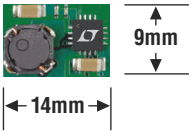


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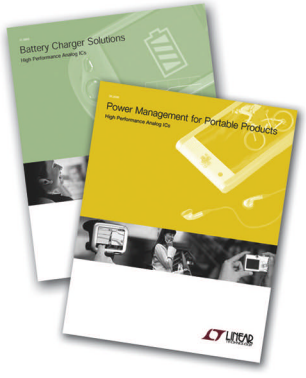


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# Soft limiter for oscillator circuits uses emitter-degenerated differential pair

Herminio Martínez and Encarna Garcia,
Technical University of Catalonia, Barcelona, Spain

Most oscillator circuits include a nonlinear amplitude control that sustains oscillations at a desired amplitude with minimum output distortion. One approach uses the output sinusoid's amplitude to control a circuit element's resistance, such as that of a JFET operating in its triode-characteristics region. Another control method uses a limiter circuit that allows oscillations to grow until their amplitude reaches the limiter's threshold level. When the limiter operates, the output's amplitude remains constant. To minimize nonlinear distortion and output clipping, the limiter should exhibit a "soft" characteristic.

Based on a waveform shaper that imposes a soft limitation or saturation characteristic, the circuit in **Figure 1** comprises a simple RC (resistor-capacitor)-ladder phase-shift oscillator and an amplitude-control limiter circuit. $R_1$, $R_2$, and $R_3$ have values of 10 kΩ each, and $C_1$, $C_2$, and $C_3$ have values of 1 nF each. The following **equation** defines output voltage $V_{OUT}$'s frequency, $f_O$.

$$f_O = \frac{\sqrt{6}}{2\pi RC} = \frac{\sqrt{6}}{2\times\pi\times 10\ \text{k}\Omega\times 1\ \text{nF}} \approx 39\ \text{kHz}.$$

The inverting-amplifier block in **Figure 1** comprises transistors $Q_1$ and $Q_2$, a differential pair that presents a nonlinear-transfer characteristic, plus an IVC (current-to-voltage converter) based on operational amplifier $IC_1$. For oscillation to occur, the inverting amplifier's gain magnitude must exceed 29. Selection of appropriate values of bias current, $I_{EE}$; the transistor pair's emitter-degeneration resistances, $R_{E1}$ and $R_{E2}$; and $R_{E3}$ produces the amplifier's nonlinear-transfer characteristic, $V_{OUT}$ versus $V_{IN}$ (**Figure 2**).

A small input voltage produces a nearly linear-amplifier-transfer characteristic. However, large values of input voltage drive $Q_1$ and $Q_2$ into their nonlinear region, reducing the amplifier's gain and introducing a gradual bend in the transfer characteristic. A current mirror comprising $Q_3$ and $Q_4$ converts the shaping circuit's output

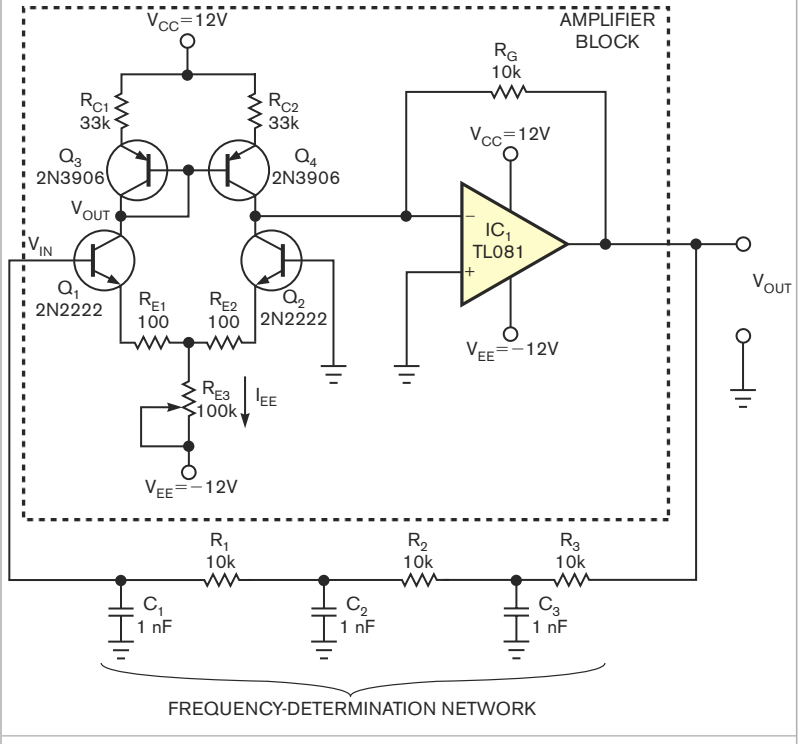


Figure 1 A phase-shift RC-oscillator circuit uses an emitter-coupled amplitude limiter.

to a single-ended current, which operational amplifier $IC_1$ converts to an output voltage. In the prototype circuit, calibration trimmer $R_{E3}$ has a value of approximately 33 kΩ. **Figure 3** shows the oscillator's output voltage for the component values in **Figure 1**, and **Figure 4** shows the sinusoidal output's spectral purity.

The nonlinear amplifier's wave-shaping action occurs independently of frequency, and this circuit offers convenience for use with variable-frequency oscillators. Note that $IC_1$'s gain-bandwidth product limits the circuit's performance. To use the limiter portion of the circuit with a noninverting amplifier, such as a Wien-bridge oscillator, apply the signal input voltage to $Q_2$'s base, and ground $Q_1$'s base.EDN

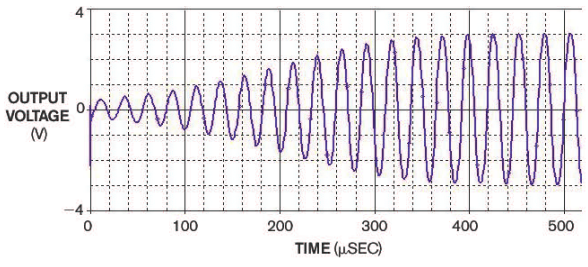


Figure 3 For the component values in Figure 1, the oscillator's output voltage reaches full amplitude in approximately 400 μsec, or 15 cycles after start-up.

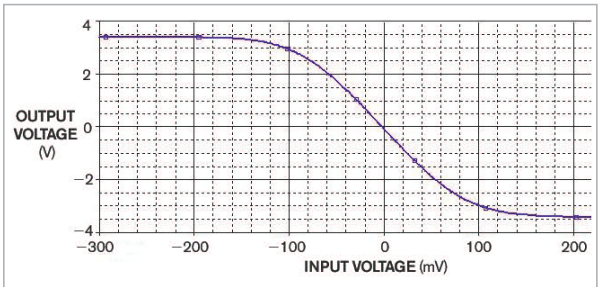


Figure 2 The transfer-characteristic output voltage versus input voltage for the nonlinear amplifier shows a gradual onset of limiting at approximately 100-mV input.

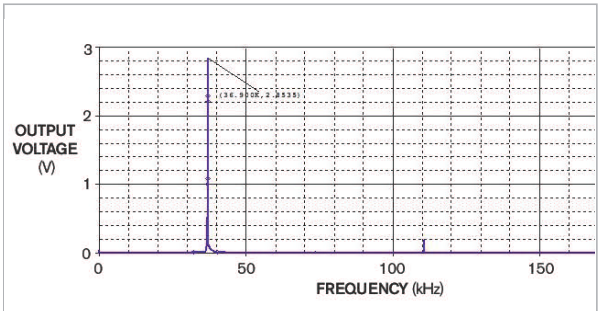


Figure 4 The oscillator's output spectrum shows only a slight amount of third-harmonic output.

# Feedback circuit enhances phototransistor's linear operation

JC Ferrer and A Garrigós, University Miguel Hernández, Elche, Spain

A designer who uses a phototransistor to convert a modulated optical signal to an electrical signal frequently encounters problems when high-intensity background light saturates the phototransistor. When its base terminal floats, a phototransistor's collector-to-emitter voltage depends only on the photocurrent generated by the superposition of the signal and background light. The phototransistor's gain and its active-region range depend on $R_1$'s resistance. For higher values of $R_1$, the circuit's gain increases, but the phototransistor saturates more quickly. In **Figure 1**, without background illumination, the transistor operates in its linear region at bias point $\phi_2$, and $Q_1$'s collector voltage varies linearly

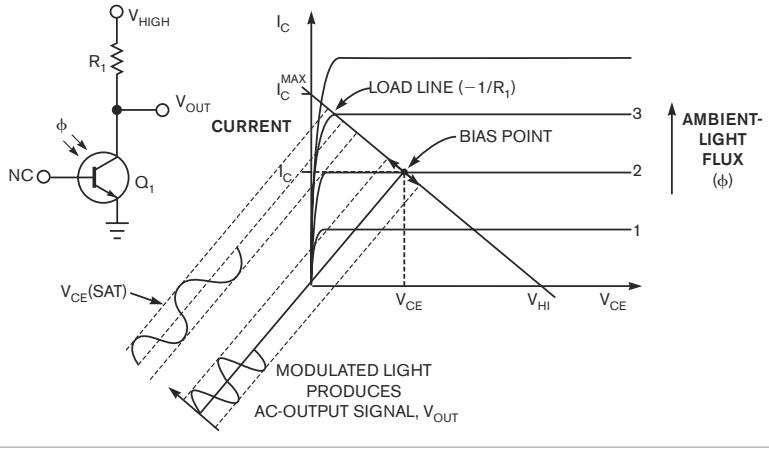


Figure 1 Varying levels of ambient-light flux affect the bias point of a basic phototransistor circuit. Higher levels force the bias point closer to saturation and compress the desired signal, $V_{OUT}$.

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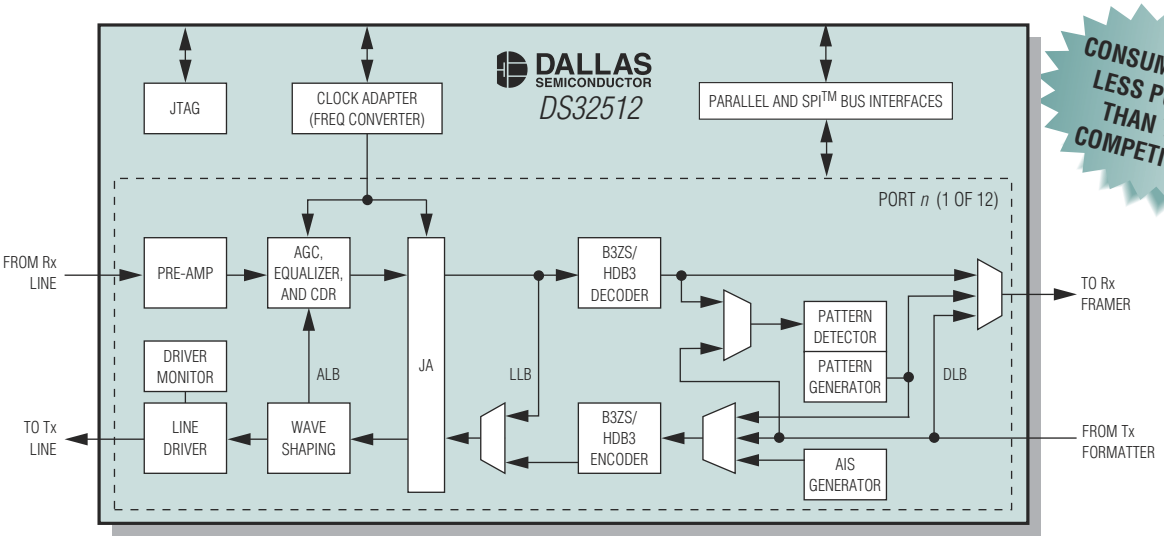


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around $V_{CE}$. Its output, $V_{OUT}$, faithfully reproduces ampltude fluctuations in the modulated optical signal. Applying extraneous steady-state background illumination shifts the circuit's operating point to bias point $\phi_3$, and the output voltage compresses and distorts.

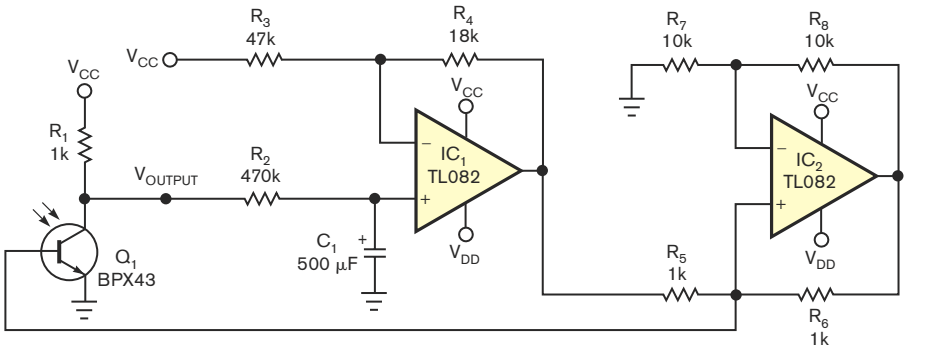


Figure 2 A feedback circuit consisting of a single-pole lowpass active filter and a Howland source diverts current from the phototransistor's base to avoid saturation at excessive background-light levels.

Unlike photodiodes and photovoltaic cells that have only two leads, a phototransistor's base connection allows a feedback circuit to control the device's bias point. Diverting current from the base terminal reduces collector current. In **Figure 2**, phototransistor $Q_1$ detects an optical signal plus background light that illuminates its base region. A lowpass active filter samples the collector voltage generated by the background light, and a Howland current source alters the circuit's bias point by draining current from the phototransistor's reverse-biased collector-base junction.

In general, extraneous background illumination fluctuates more slowly than the desired signal. For simplicity, this design uses a first-order lowpass filter, $C_1$ and $R_2$, with a cutoff frequency below the signal frequency to sample $Q_1$'s collector voltage. Applying a reference voltage—$V_{CC}$, in this example—to $R_3$ sets the filter circuit's dc operating point midway between the phototransistor's cutoff and saturation voltages. The lowpass filter's output drives a Howland current source to produce a current proportional to the filter's output. As background illumination increases, $Q_1$'s collector voltage decreases. The current source's output subtracts from $Q_1$'s base current, which in turn raises $Q_1$'s collector voltage to avoid saturation.

The ratio of $R_4$ to $R_3$ establishes the active lowpass filter's gain according to the equation $A_V=1+(R_4/R_3)$, and $R_5$ sets the current source's transconductance: $G_M=1/R_5$. Altering these resistors affects the amount of current drained from the phototransistor's base and the circuit's operating point. The phototransistor has much lower capacitance than the filter, ensuring that the circuit in **Figure 2** cannot oscillate. However, replacing the first-order lowpass filter with a second-order lowpass filter requires careful selection of the capacitors' values to avoid oscillation.

Illuminating the phototransistor with a 100W incandescent light bulb provides high-intensity-light background lighting plus a rapidly changing signal due to the applied ac-line

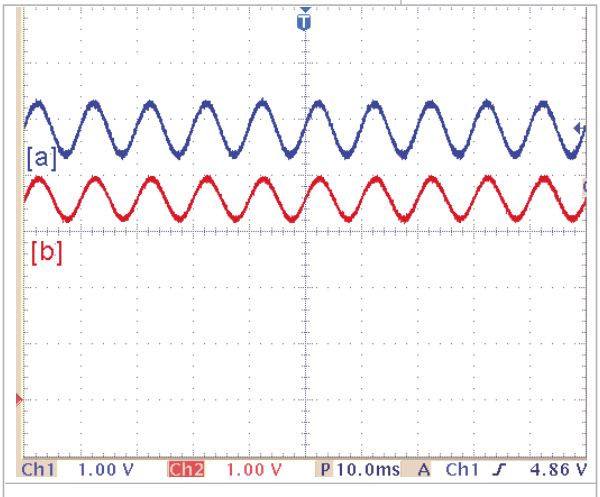


Figure 3 A 100W light bulb at a 40-cm distance illuminates a collector-emitter voltage of a phototransistor with a feedback circuit (a) and with no feedback (b). Both bias points remain in the linear region.

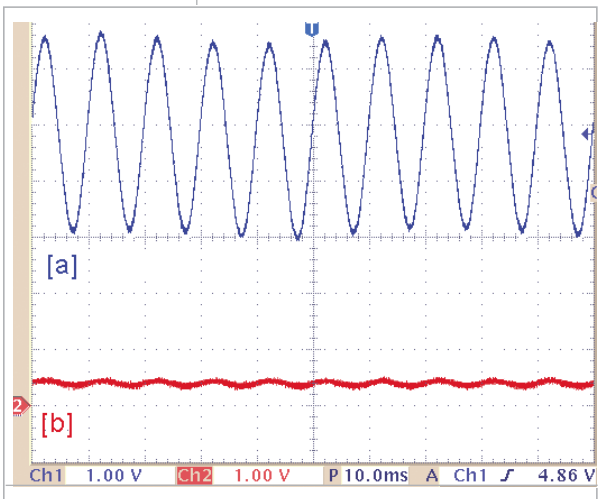


Figure 4 A 100W light bulb at a 20-cm distance illuminates the collector-emitter voltage of a phototransistor with a feedback circuit (a) and with no feedback (b). Saturation of the circuit with no feedback prevents signal detection.

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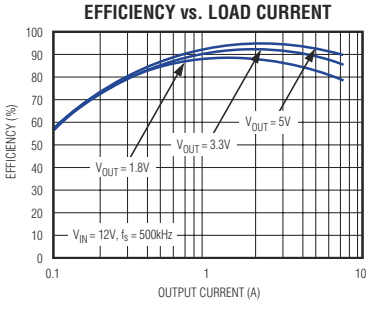


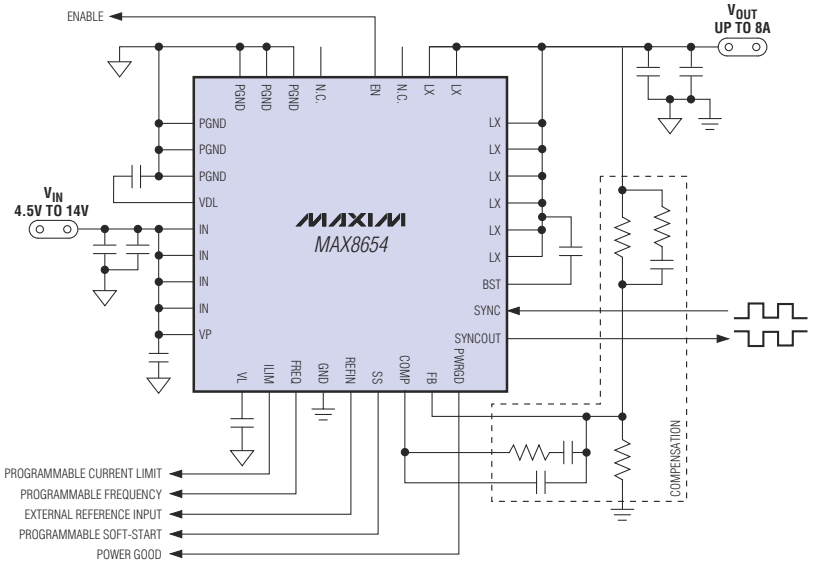


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voltage. **Figure 3** shows $Q_1$'s collector-to-emitter voltage with the light bulb 40 cm from the phototransistor with the feedback circuit active (**Figure 3a**) and for the circuit with the phototransistor's base floating (**Figure 3b**). The responses appear similar because the phototransistor doesn't saturate at the applied light intensity.

Repositioning the light bulb at 20 cm from the phototransistor increases the background-light level and drives the phototransistor closer to saturation. When you apply feedback, the phototransistor delivers a higher amplitude signal, although its bias point remains almost unchanged (**Figure 4a**). The average dc-voltage level at $Q_1$'s collector remains almost the same as at the lower light level (**Figure 3a**). However, with no feedback applied, the phototransistor's bias point moves close to saturation, and the ac-modulated light variations are barely detectable (**Figure 4b**). EDN

# Three-phase sinusoidal-waveform generator uses PLD

Eduardo Perez-Lobato, University of Antofagasta, Antofagasta, Chile

Using the circuit in this Design Idea, you can develop and implement a lightweight, noiseless, inexpensive, three-phase, 60-Hz sinusoidal-waveform voltage generator. Although targeting use as a circuit for testing power controllers, it can serve other applications that require three sine waves with a 120° relative phase difference. A 22V10 PLD (programmable-logic device) at $IC_1$ generates three three-phase, 60-Hz, square-wave voltages. Internal register $IC_1$ and $Q_0$, $Q_1$, and $Q_2$ bits set the

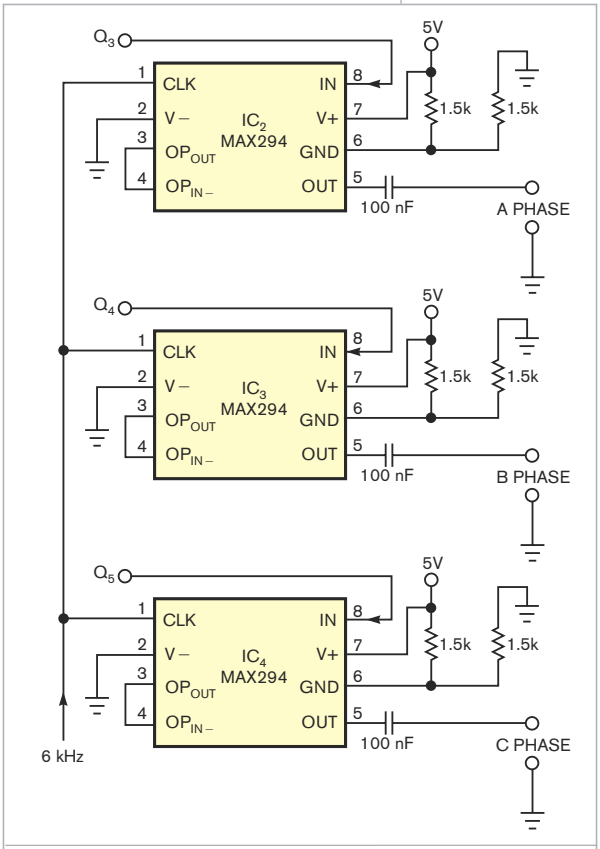


Figure 2 Switched-capacitor filters remove all but the sinusoidal fundamental signal from the PLD's three-phase square-wave outputs.

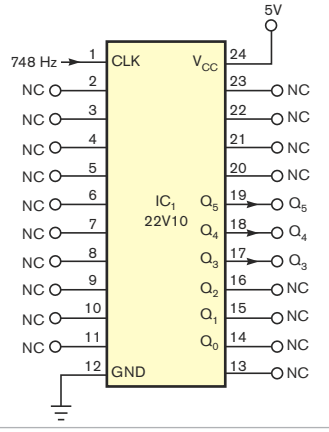


Figure 1 An external 748-Hz clock source drives this PLD-based, three-phase sine-wave generator.

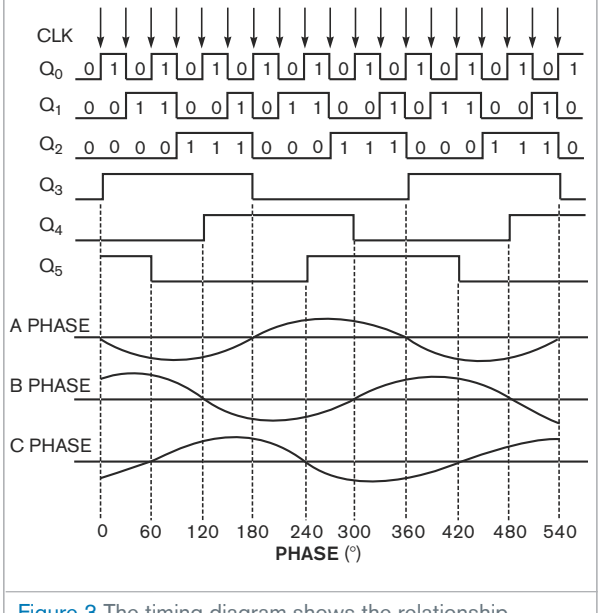


Figure 3 The timing diagram shows the relationship between the clock and the three-phase outputs.

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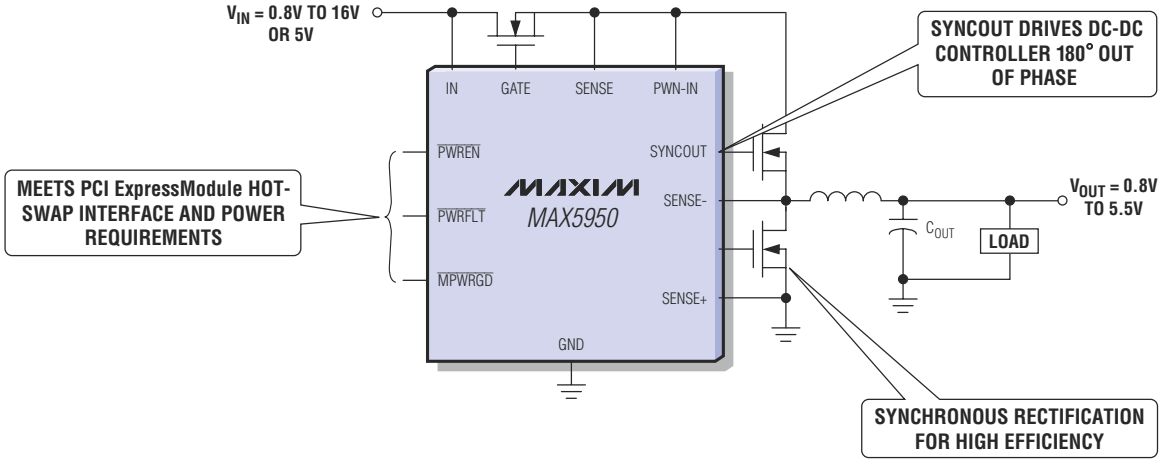


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$Q_3$ bit to lead the $Q_4$ bit by 120° and set the $Q_5$ bit to lag behind the $Q_3$ bit by 240° (**Figure 1**). Setting $IC_1$'s clock frequency to 748 Hz produces 60-Hz outputs at $Q_3$, $Q_4$, and $Q_5$.

$IC_1$'s three square-wave output voltages—$Q_3$, $Q_4$, and $Q_5$—drive $IC_2$, $IC_3$, and $IC_4$, three Maxim (www.maxim-ic.com) MAX294 eighth-order, low-pass, switched-capacitor filters to produce three 2V sinusoidal waveforms (**Figure 2**). When you connect $IC_5$, a common 555 timer as an astable oscillator, it produces a 6-kHz, TTL-level source that clocks all three filters at 100 times the desired 60-Hz output frequency. A 100-nF dc-blocking capacitor at each filter's output ensures that the three-phase outputs swing from +2 to −2V with respect to ground. Note that each filter inverts its output and introduces a 180° phase shift with respect to its input square wave.

**Figure 3** depicts the phase relationships among $IC_1$'s outputs and yields Boolean equations (**Table 1**). The equations translate into set/reset signals that produce 64 logic states when you apply them to a 6-bit sequencer block in $IC_1$. Outputs $Q_5$, $Q_4$, and $Q_3$ represent the three most-significant bits, and $Q_2$, $Q_1$, and $Q_0$ represent the three least-significant bits. After translation, an emulated Basic program (**Listing 1**), which you can download from www.edn.com/061012di1, produces fuse-programming code for $IC_1$'s sequencer and logic states. Although only 16 logic states define the sequencer's functions, its remaining 48 states also require definition to avoid anomalous operation. EDN

**TABLE 1 BOOLEAN EQUATIONS**

| | |
|---|---|
| $SET\_Q_0=\overline{Q_0}$ | $RESET\_Q_0=Q_0$ |
| $SET\_Q_1=\overline{Q_1}\times Q_0$ | $RESET\_Q_1=\overline{Q_2}\times Q_1\times\overline{Q_0}+Q_2\times Q_1\times\overline{Q_0}$ |
| $SET\_Q_2=\overline{Q_2}\times Q_1\times\overline{Q_0}$ | $RESET\_Q_2=Q_2\times Q_1\times\overline{Q_0}$ |
| $SET\_Q_3=\overline{Q_3}\times Q_2\times Q_1\times\overline{Q_0}$ | $RESET\_Q_3=Q_3\times Q_2\times Q_1\times\overline{Q_0}$ |
| $SET\_Q_4=\overline{Q_4}\times Q_2\times\overline{Q_1}\times\overline{Q_0}$ | $RESET\_Q_4=Q_4\times Q_2\times\overline{Q_1}\times\overline{Q_0}$ |
| $SET\_Q_5=\overline{Q_5}\times\overline{Q_2}\times Q_1\times\overline{Q_0}$ | $RESET\_Q_5=Q_5\times\overline{Q_2}\times Q_1\times\overline{Q_0}$ |

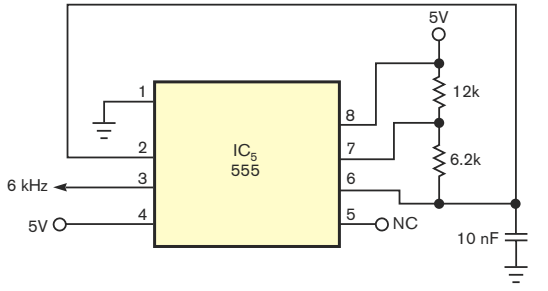


Figure 4 A garden-variety 555 timer IC provides a 6-kHz clock for the switched-capacitor filters.

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DESIGN NOTES

# True Rail-to-Rail, High Input Impedance ADC Simplifies Precision Measurements – Design Note 400

Mark Thoren

## Introduction

High input impedance and a wide input range are two highly desirable features in a precision analog-to-digital converter, and the LTC®2449 delta-sigma ADC has both. With just a few external components, the LTC2449 forms an exceptional measurement system with very high input impedance and an input range that extends 300mV beyond the supply rails.

A designer may trade off the LTC2449's 200nV resolution for faster conversion rates, but otherwise the LTC2449 requires few to no performance tradeoffs. It simultaneously achieves 1ppm linearity (Figure 2), 200nV input resolution and a 5V input span. Ten filter oversample ratios are available, providing data rates from 6.8 samples per second to 3500 samples per second. Normal mode rejection of 50Hz and 60Hz is better than 87dB in the 6.8sps mode. *All DC specifications hold for all speeds*—only the resolution changes. Such persistent high performance simplifies the design of otherwise challenging applications, such as 6-digit voltmeters, sensor interfaces, and industrial control. In addition, the LTC2449 digital interface and timing are extremely simple, and the No Latency architecture eliminates concerns about filter settling when scanning multiple input channels.

## Solving Common Issues

One unique feature of the LTC2449 is that the analog inputs are routed to the MUXOUT pins, and an external buffer isolates these signals from the switched capacitor ADC inputs (See Figure 1). The external buffer yields high impedance through the multiplexer and back to the analog inputs. This has a distinct advantage over integrated buffers because the analog inputs are truly rail-to-rail, and slightly beyond, with appropriate buffer supply voltages.

The LTC6241 is a precision CMOS amplifier with 1pA bias current and impressive DC specifications: the maximum offset is 125µV and the open loop gain is 1.6 million,



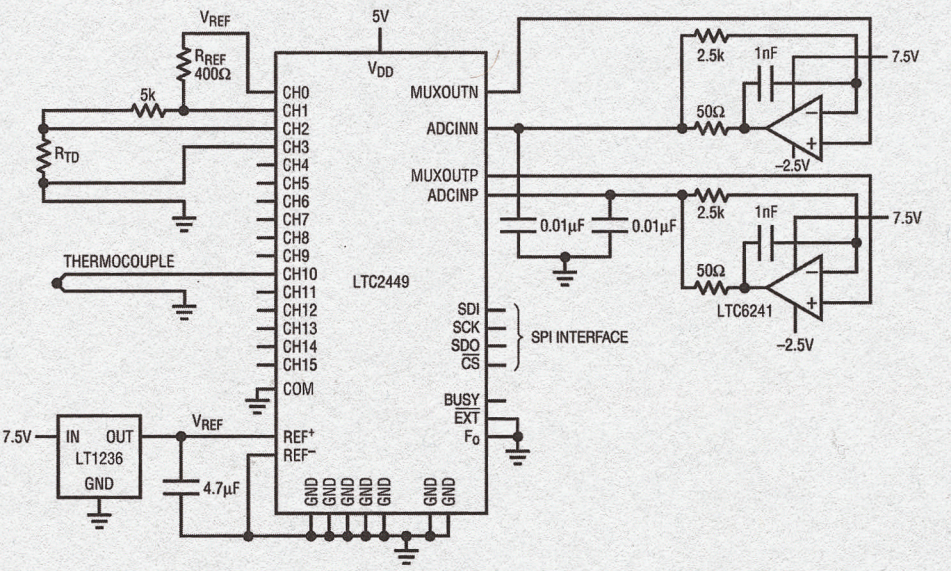


**Figure 1. Temperature Sensing Application Example**

typical. While the offset is not important in this application because it is removed by the LTC2449's multiplexer switching technique, the high open loop gain ensures that the 10ppm typical gain error of the LTC2449 does not degrade. Figure 1 shows proper interfacing of the LTC6241 to the LTC2449. The amplifier's 0.01µF capacitive load and compensation network provides the LTC2449 with a charge reservoir to average the ADC's sampling current while the 2.5k feedback resistor maintains DC accuracy.

The LTC6241 has a rail-to-rail output stage, and an input common mode range from the negative supply to 1.5V lower than the positive supply. Since no rail-to-rail amplifier can actually pull its outputs to the rails, an LT3472 boost/inverting regulator is used to create the –2.5V and 7.5V op amp supplies from the 5V supply as shown in Figure 3. This regulator can provide enough current for several amplifiers and other circuitry that *really* needs to swing to the rails. In addition, the LT3472's 1.1MHz switching frequency is close to the middle of the LTC2449 digital filter stopband. The center of the stopband is 900kHz when using the internal conversion clock and is independent of the selected speed mode.

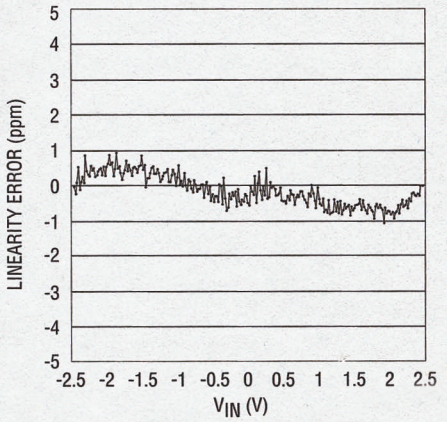


**Figure 2. LTC2449 Integral Non-Linearity**

## Applications

The LTC2449 is commonly used with thermocouples and RTDs as shown in Figure 1. Thermocouple outputs produce very small changes (tens of microvolts per degree C) and the output will be negative if the thermocouple is colder than the "cold junction" connection from the thermocouple to the copper traces on the PCB. The RTD is measured by comparing the voltage across the RTD to the voltage across a reference resistor. This provides a very precise resistance comparison and it does not require a precise current source. Grounding the sensors as shown is a good first line of defense for reducing noise pickup; however, the ADC must accommodate input signals that are very close to or slightly outside the supply rails. The LTC2449 handles these signals perfectly.

## Conclusion

The LTC2449 solves many of the problems that designers encounter when trying to apply delta-sigma ADCs in demanding applications. High impedance, rail-to-rail inputs and a very simple serial interface simplify both hardware and software design.

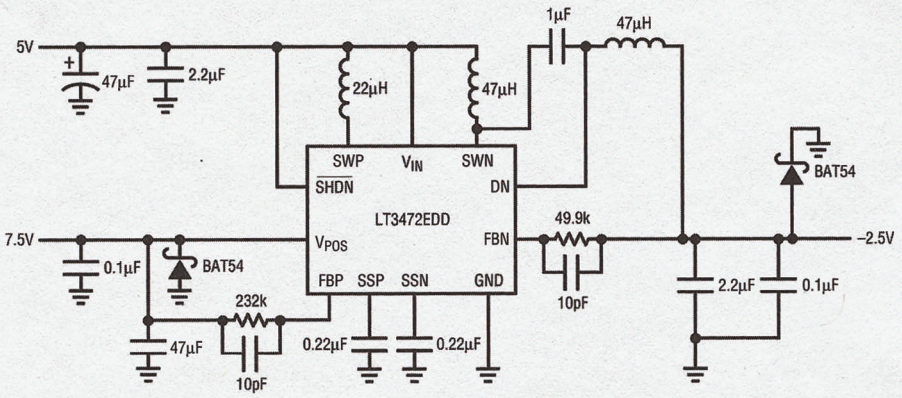


**Figure 3. Power Supply for Buffers**

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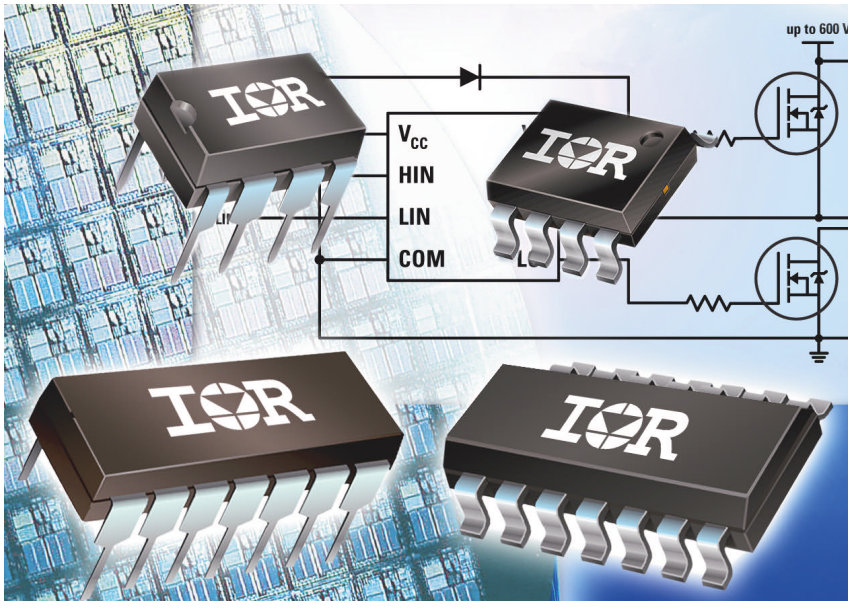


### High-voltage-IC series features undervoltage-lockout protection

This series of 19 500 and 600V high-voltage ICs, half-bridge drivers, and high- and low-side drivers targets motor control, switch-mode power supplies, and flat-panel displays. Features include single or dual inputs, undervoltage-lockout protection, fixed or programmable dead time for half-bridge drivers, and 2.5A drive currents. The high-voltage-IC technology integrates N- and P-channel low-voltage-MOS circuitry in a driver IC. A bootstrap-power-supply option eliminates the need for an auxiliary power supply. Available in surface-mount and dual-inline packages, these ICs cost $1 (10,000).

**International Rectifier, www.irf.com**

## Power MOSFETs come in tiny packaging

Adding to the vendor's line of power-management devices, the uPA2350 and uPA2351 power MOSFETs measure 1.62×0.48 mm, reducing the typical footprint by as much as 86% compared with TSSOP-8 packages. Targeting dual N-channel MOSFETs for battery-protection applications, the devices suit use in lithium-ion-battery packs in portable applications. The uPA2350 and uPA2351 feature 28- and 32-mV on-state resistance for extended battery life. The devices cost 35 cents (10,000).

**NEC Electronics, www.am.necel.com**

## MOSFET/IGBT driver eliminates need for a negative gate driver

The 1V-maximum low-level output voltage in the VO3150 0.5A MOSFET/IGBT (integrated-gate-bipolar-transistor) driver eliminates the need for a negative gate driver. Combining a high-speed optocoupler and an IGBT/MOSFET driver in one package, this isolated device suits direct driving of IGBTs with 1200V and 50A ratings in industrial and consumer applications. Features include a 5300V-rms isolated voltage; minimum and typical common-mode rejection of 15 and 30 kV/µsec, respectively; and a 1500V common-mode voltage. Available in a DIP-8 package, the VO3150 costs $1.93 (10,000).

**Vishay Intertechnology, www.vishay.com**

## Medium-current, high-voltage diodes come in compact packages

The UFHV high-voltage-diode family features a 30A maximum-surge current. A DO-41 package suits the devices for medium-power, high-voltage power supplies. The 2000V/850-mA UFHV2K, the 3000V/825-mA UFHV3K, and the 4000V/800-mA UFHV4K cost 25, 35, and 45 cents (1000), respectively.

**HV Component Associates, www.hvca.com**

## SuperFET devices reduce on-resistance by one-third

The 600V Dpak SuperFET MOSFETs suit ultraslim, low-profile ballast-application requirements. Features include a 0.6Ω on-resistance, compared with a typical 1.2Ω on-resistance of traditional planar MOSFETs, and the ability to withstand high-speed voltage- and current-switching transients. The FCD7N60 SuperFET costs $1.54.

**Fairchild Semiconductor, www.fairchildsemi.com**



## MOSFET driver claims high power efficiency

Targeting server and dc/dc-power systems, the high-speed, synchronous, 4A TPS28225 MOSFET driver features 14-nsec adaptive dead-time control, 14-nsec propagation delays, a 2A source drive, and a 4A sink drive. Suiting N-channel complementary-driven power MOSFETs, the driver controls MOSFET gates with 4.5 to 8.8V, and the vendor claims a 7 to 8V power efficiency. A 0.4Ω impedance for the lower gate driver holds the gate of the power MOSFET below its threshold level, ensuring no shoot-through current occurs during high dV/dT phase-node transitions. An internal diode charges a bootstrap capacitor, allowing the use of N-channel MOSFETs in half-bridge configurations. Available in SOIC-8 and thermally enhanced 3×3-mm DFN-8 packages, the TPS28225 costs 60 cents (1000).

**Texas Instruments, www.ti.com**

# MICROPROCESSORS

## Microcontrollers feature 650-nA power consumption

The 44-pin ATmega164P, ATmega324P, and ATmega644P AVR general-purpose microcontrollers incorporate the vendor's picoPower technology, reducing power consumption to as little as 650 nA with the 32-kHz clock running, 340 µA in active mode, 650 nA in power-save mode with a real-time counter, and 100 nA in power-down mode. The devices features 16, 32, and 64 kbytes, respectively, of self-programmable flash program memory; each also has a 10-bit ADC, two USARTs, an SPI, and a two-wire interface. The microcontrollers can operate from 1.8 to 5.5V. The devices feature pin-compatible performance and are code-compatible with other AVR microcontrollers. The units sell for $2.23, $2.78, and $3.72 (10,000), respectively.
**Atmel Corp, www.atmel.com**

## Dual-core processor features socket AM2 compatibility

Compatible with socket AM2, the Athlon 62 X2 dual-core processor 5200+ enables the vendor's virtualization technology and high-performance, unbuffered DDR2 memory. The Athlon 64 X2 costs $403 (1000).
**AMD, www.amd.com**

## Processor features integrated security-hardware acceleration

The MPC8533E PowerQuicc III processor features a 256-kbyte L2 cache and an e500v2-core operating as fast as 1 GHz. The processor integrates security-hardware acceleration to support the pending IEEE P2600 standard from the hard-copy-device and system-security working group. The device's high-speed serial interface supports the high-bandwidth PCI Express open standard and Gigabit Ethernet. The hardware-acceleration engine includes a double-precision, floating-point, signal-processing engine; TCP (Transfer Control Protocol) offloading; and a security-acceleration engine. The MPC8533 without encryption and the MPC8533E with encryption, employing 90-nm-process technology, are available in 783-pin FC-PBGA packages. The MPC8533 with 400-MHz will be available in the fourth quarter of 2007, and prices will start at $64.79 (10,000).
**Freescale Semiconductor, www.freescale.com**

## Microcontroller core has an expandable address space

Based on the TLCS-870/C architecture, the 8-bit TLCS-870/C1 microcontroller core can process one instrument cycle in a single clock cycle. A memory-management method manages code and data in separate areas, making possible an expandable address space as large as 128 kbytes. The device is binary-compatible with the vendor's previous 8-bit microcontrollers.
**Toshiba America Electronic Components, www.chips.toshiba.com**

## Development kit comes with a form-factor reference board

Targeting Microsoft's Windows Vista Sideshow platform and .NET Micro Framework, the i.MXS development kit features a form-factor reference board with a 2.5-in. color LCD panel with QVGA resolution. The card includes the vendor's i.MXS applications processor, a USB interface, and an expansion connector for add-on modules, including Bluetooth technology or ZigBee wireless protocol. The i.MXS development kit costs $499.10.
**Freescale Semiconductor, www.freescale.com**

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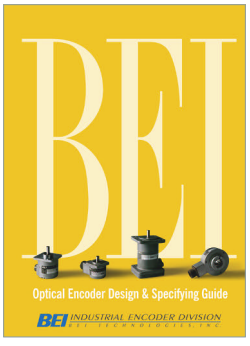
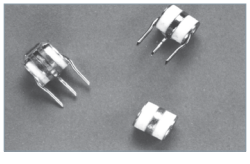
## DESIGN GUIDE FOR OPTICAL ENCODERS




This Guide provides a comprehensive summary of optical encoders, accessories and interface electronics. Included are design examples, absolute and incremental encoders, shafted and hollow-shaft styles as well as serial output versions. Special sections include hazardous environments. Call 1-800-ENCODER or visit our web site at www.beiied.com.

## SURGE PROTECTION



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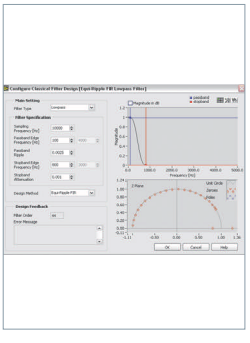

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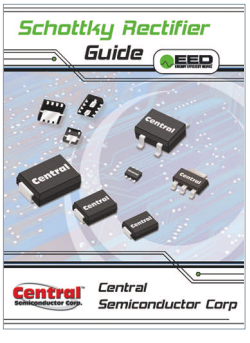


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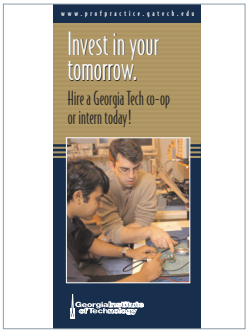


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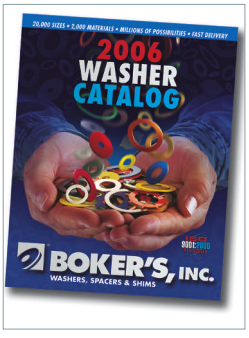


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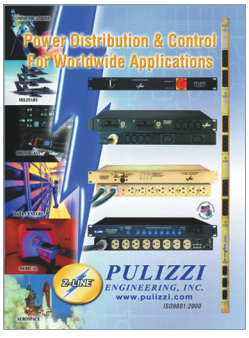


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EDITED BY RON WILSON

# scope

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## LOOKING AHEAD

### To the ATCA Summit

**From October 17 to 19 in Santa Clara, CA, the ATCA (Advanced Telecommunications Computing Architecture) Summit takes place at the Santa Clara Marriott Hotel. There was a time when telecommunications technology was about analog switching gear, microwaves, and the like. But today, it's about high-availability computing. If you are in the middle of the ATCA market, you already know this fact, and you already know about the ATCA Summit. If not, here's an opportunity to take ideas from an application that is stressing the bounds of event-driven, high-reliability computing, memory bandwidth, storage architectures, and multiprocessor-interconnect schemes. Sounds a lot like tomorrow's SOCs (systems on chips), doesn't it?**

## LOOKING BACK

**50 YEARS AGO IN *EDN***

### Solar cell cuts energy-conversion costs

Substantial reduction in the cost of manufacturing silicon solar cells promises to contribute greatly toward finding increasing applications for solar energy. Within two or three years, the cost of converting solar energy into electricity by means of the silicon solar cells should be reduced from the $600 per watt present cost to about $30 per watt. While present methods of solar-energy conversion operate at approximately 10% efficiency, in two or three years this figure should increase to a point where 15% of the sun's energy can be utilized. Potential applications for solar-energy converters … include power supplies for transistorized radio receivers and transmitters.

*—October 1956*

## LOOKING AROUND

### AT THE GROWING INFLUENCE OF PRIVATE EQUITY COMPANIES

In a trend reminiscent of the giant conglomerates of the 1970s, private-equity companies are buying into the electronics industry. In recent months, these investment ventures have picked up Avago (www.avagotech.com)—formerly, the semiconductor arm of Agilent Technologies (www.agilent.com)—and Philips Semiconductors (www.nxp.com), and rumors have swirled about Freescale Semiconductor (www.freescale.com), as well. Some say that private-equity ownership, which in principle emphasizes the old-time virtues of value and patience, is exactly what a semiconductor company needs to stay focused in a highly cyclical market. Others look back to how the conglomerate boom ended and wonder whether, once again, it's about buying up cash flows at a discount and loading them with debt to drain the value out of a viable operation. They fear layoffs and further cuts in research and development.

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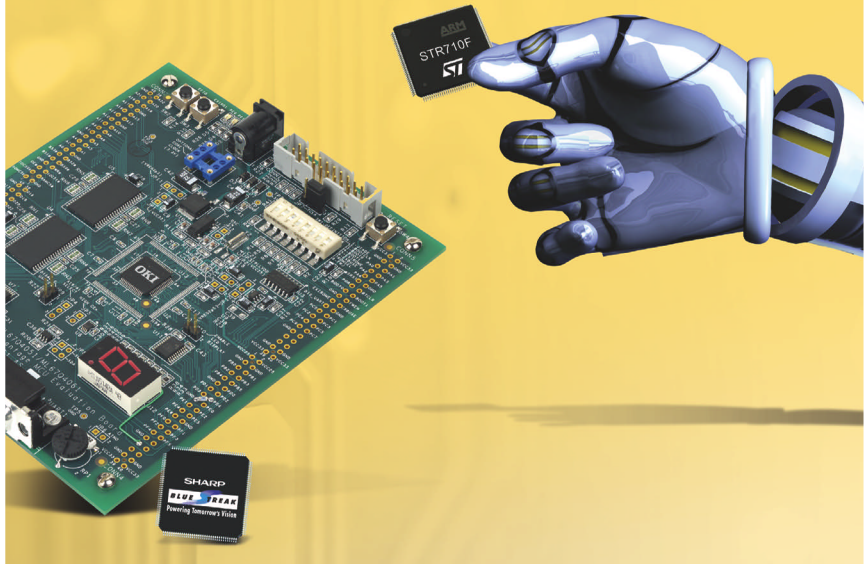


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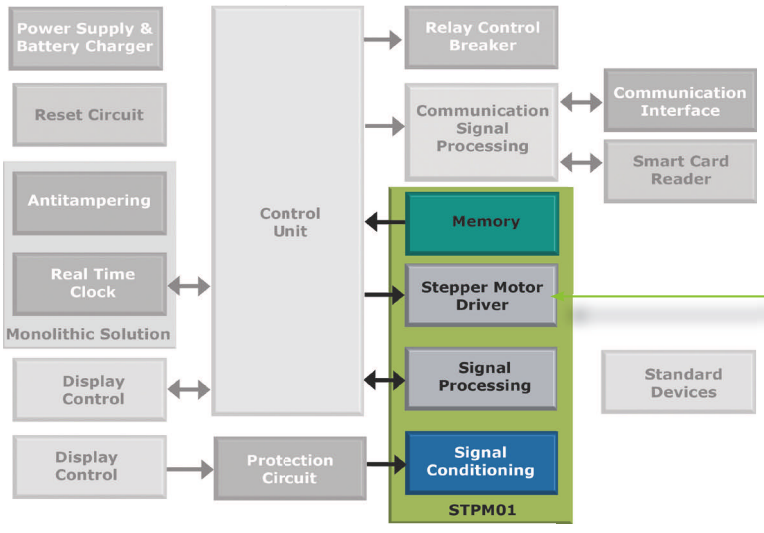


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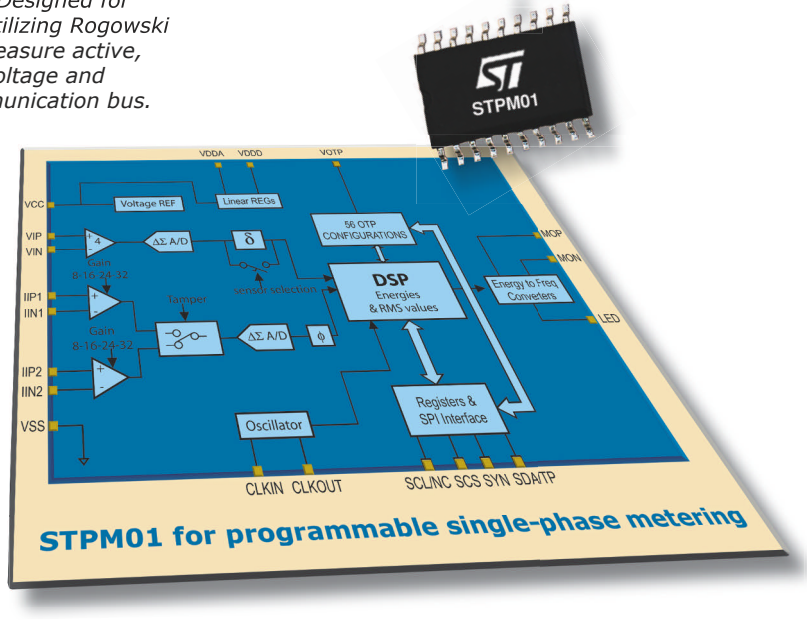


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